

Winery CALPELLA N11M-GE Schematics

Mobile Arrandale

Intel IbeX Peak-M

2010-01-18

REV : X-build

DY : Nopop Component

UMA : Pop when schematic is UMA

DIS : Pop when schematic is DIS

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
Custom

Document Number

Vostro Calpella

Rev
X01

Date: Monday, January 18, 2010

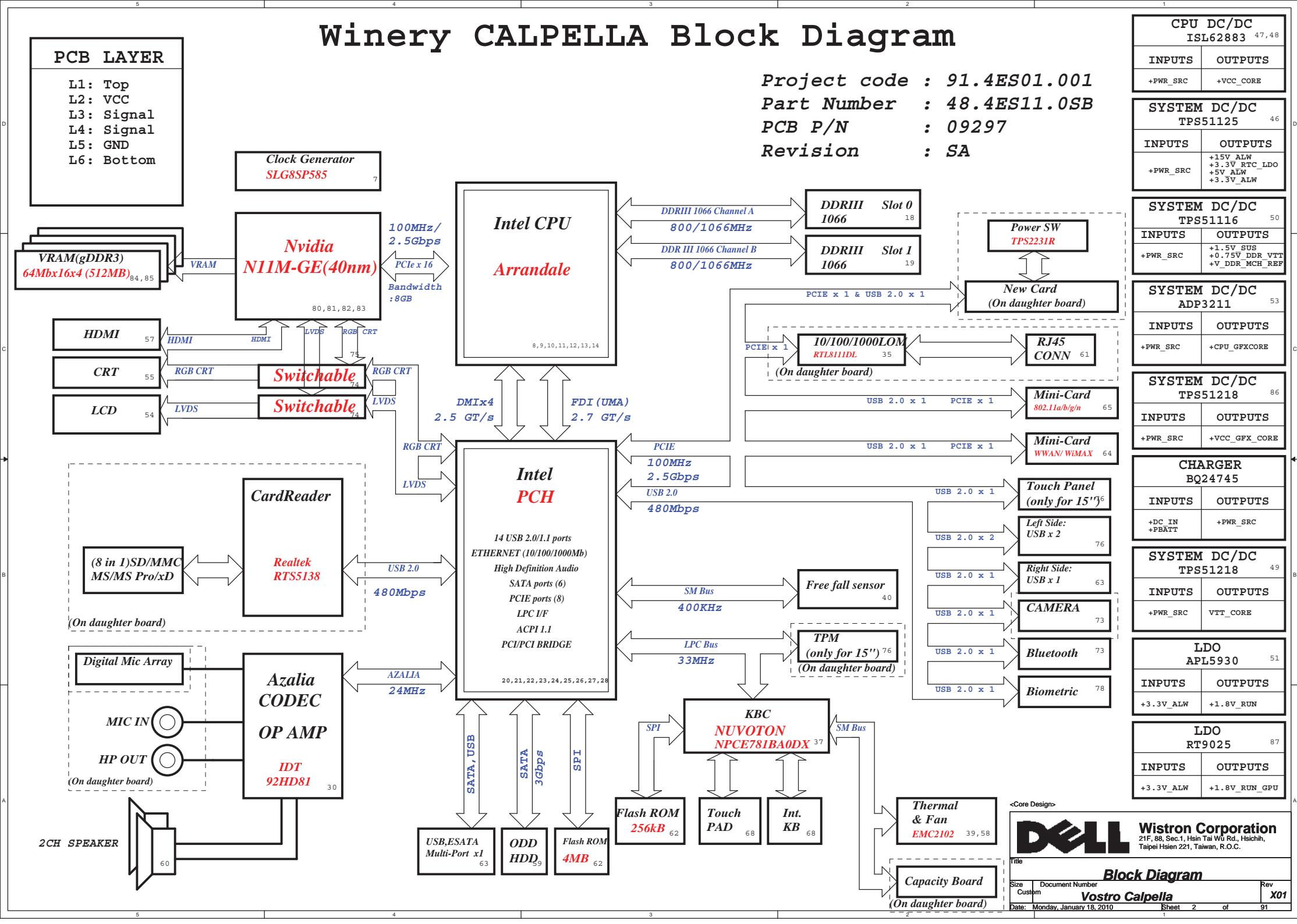
Sheet 1 of 91

Winery CALPELLA Block Diagram

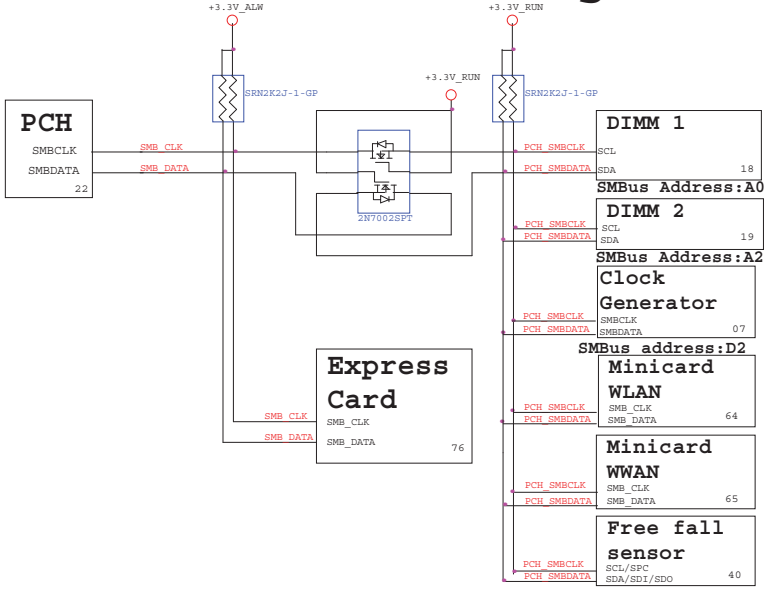
PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

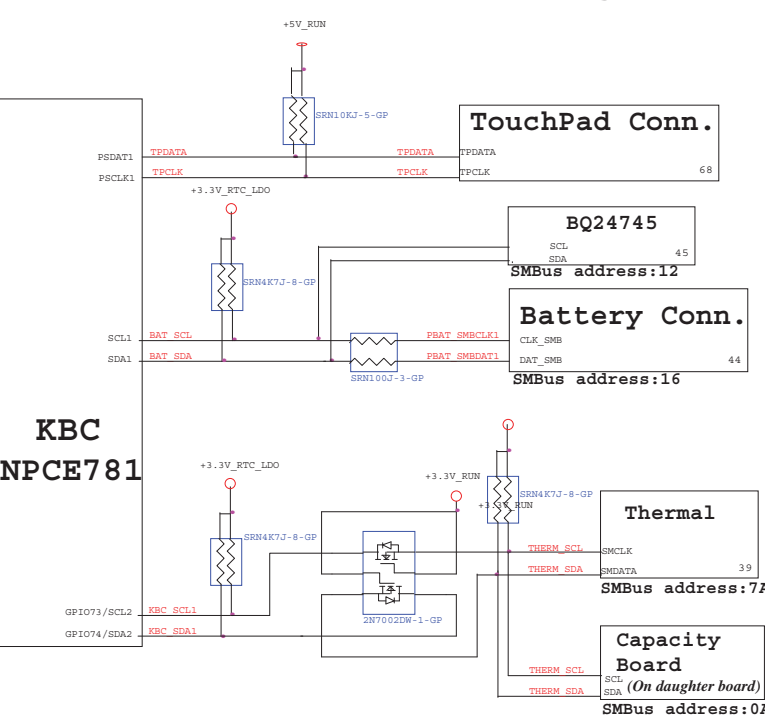
Project code : 91.4ES01.001
Part Number : 48.4ES11.0SB
PCB P/N : 09297
Revision : SA



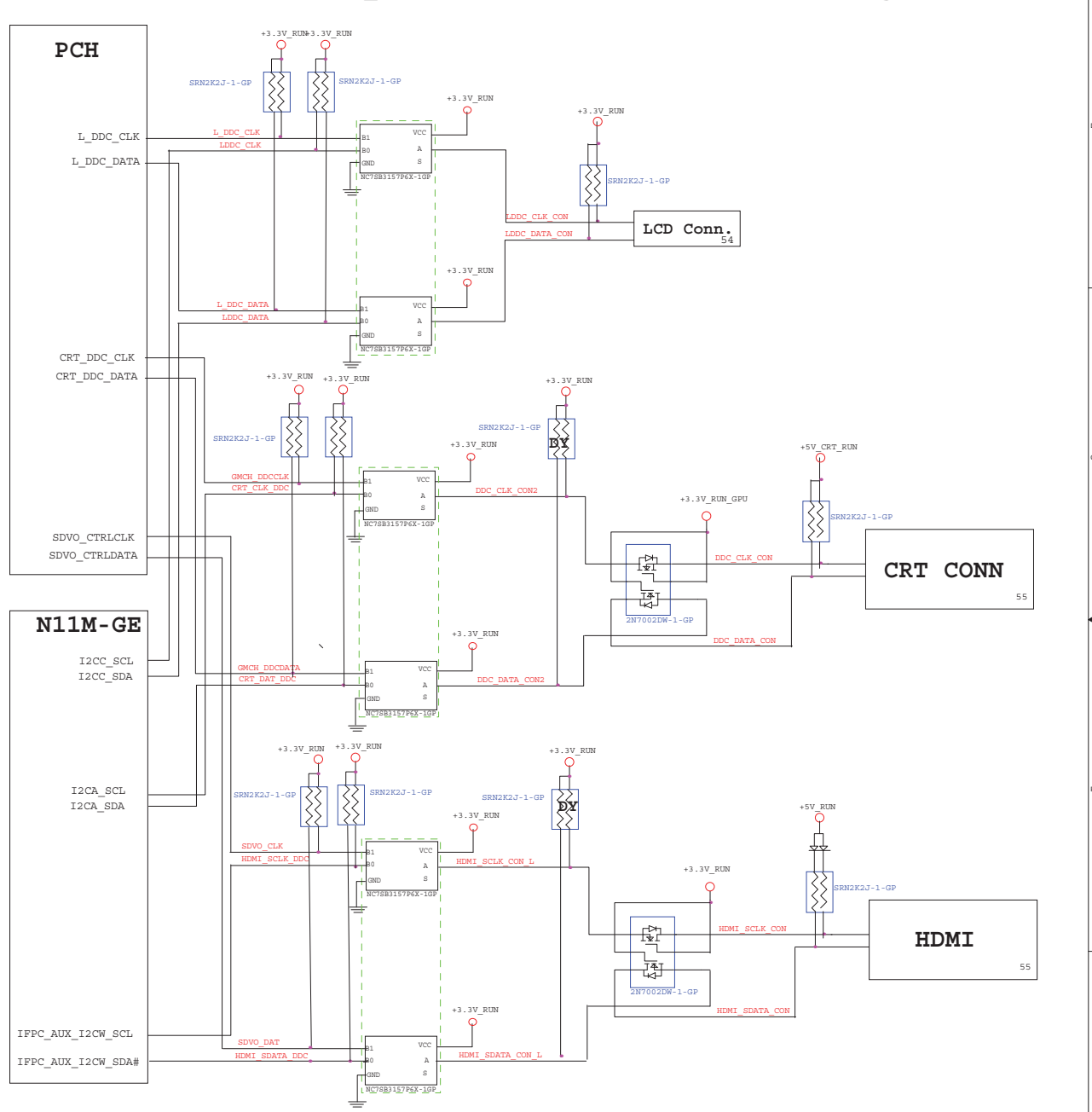
PCH SMBus Block Diagram



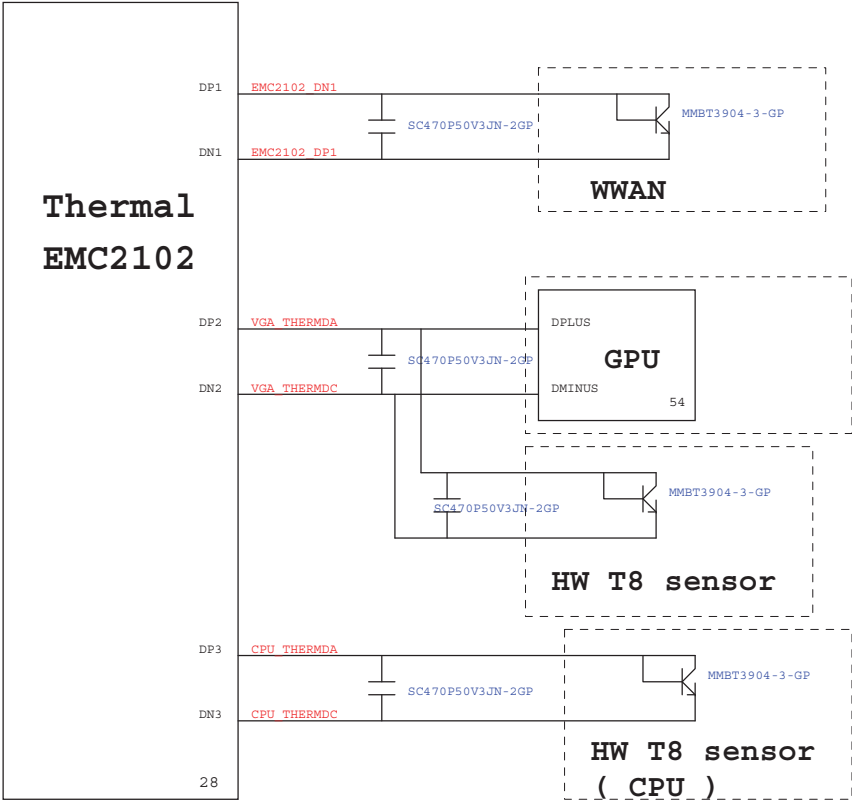
KBC SMBus Block Diagram



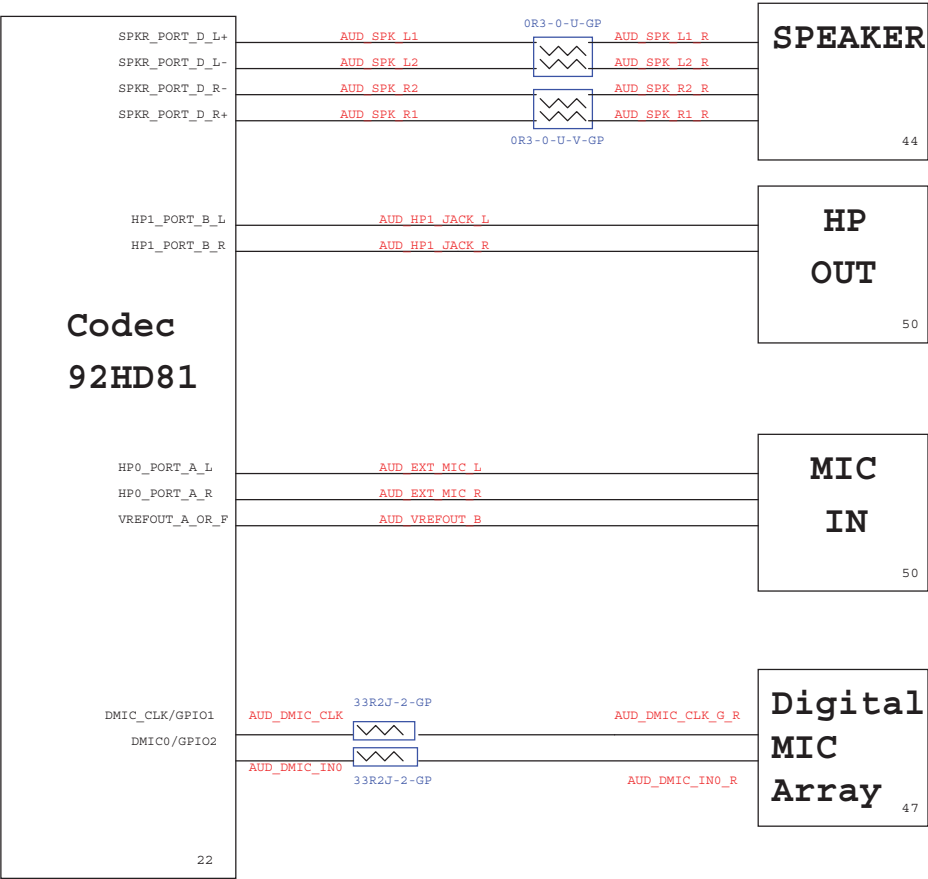
Switchable Graphic SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap ModeNote: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 k do not stuff resistor.
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Table of Content

Size

Document Number

Rev

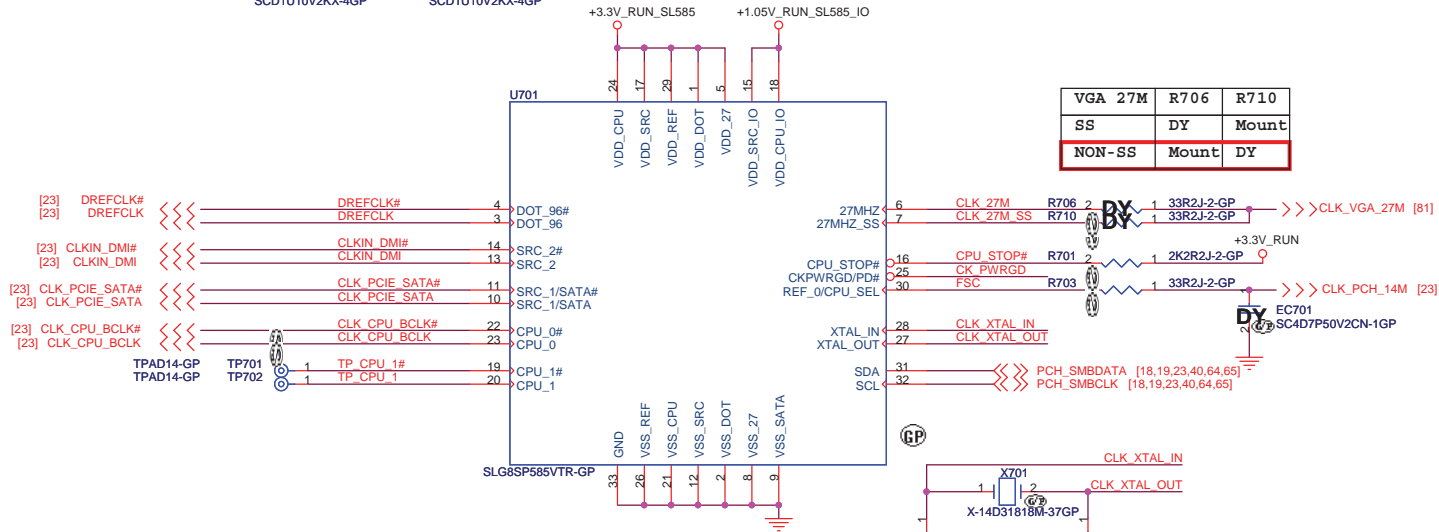
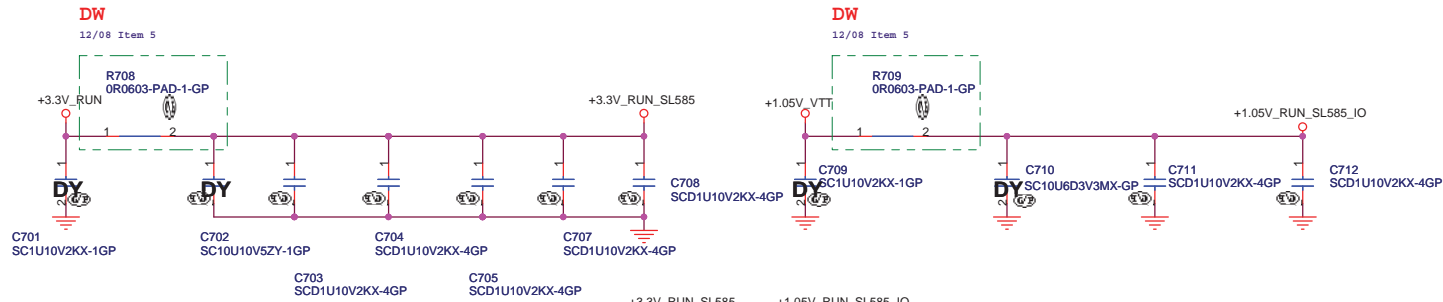
Custom

Vostro Calpella

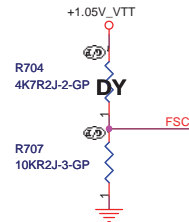
X01

Date: Monday, January 18, 2010

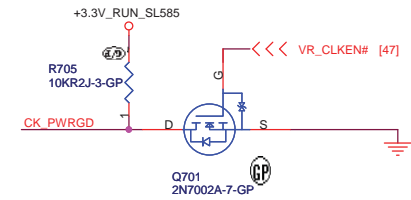
Sheet 6 of 91



1st Silego 71.08585.003
2nd ICS 71.93197.003



VGA_27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY



FSC	0	1
SPEED	133MHz (Default)	100MHz

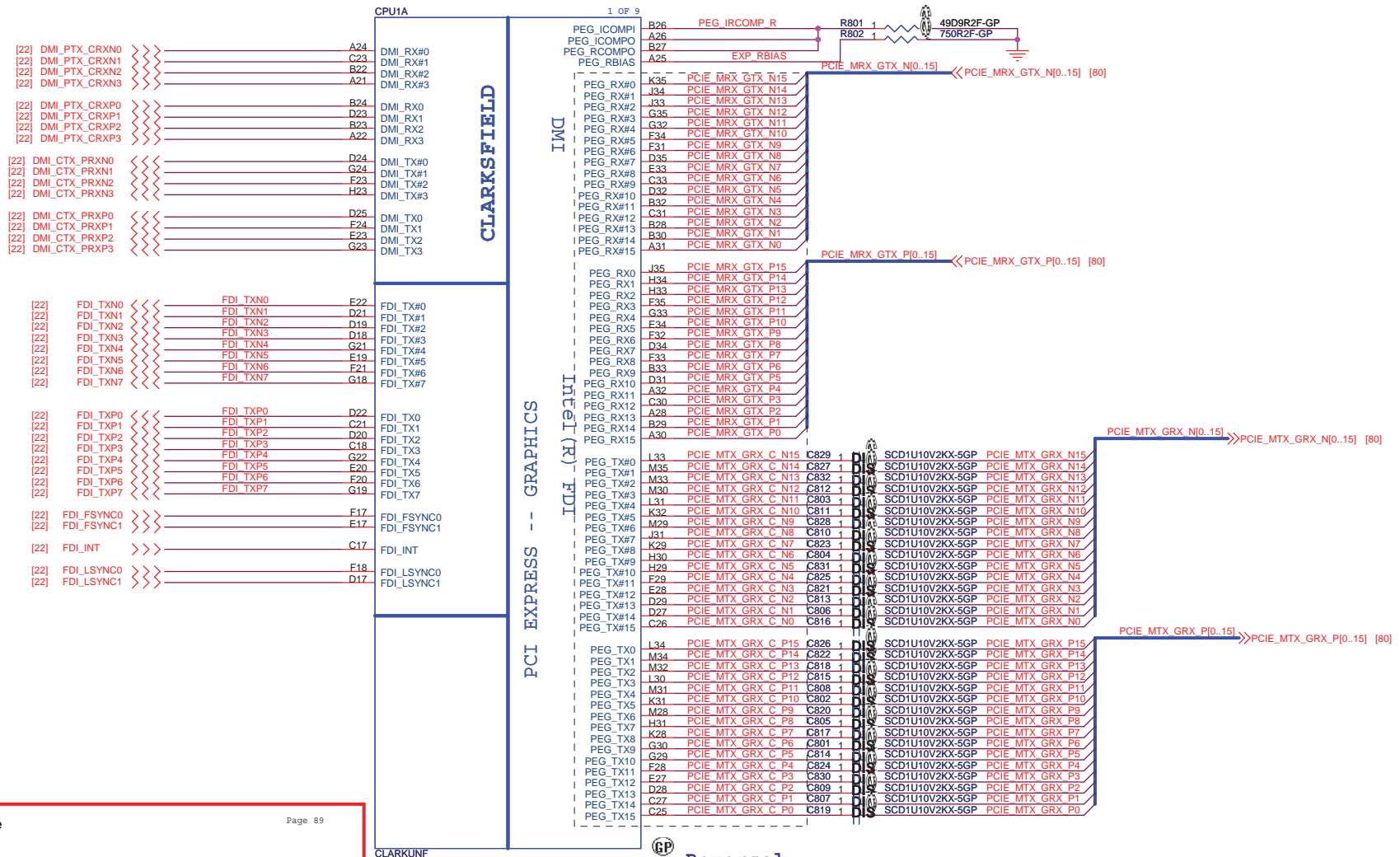
<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator SLG8SP585**

Size: Document Number Rev: **X01**

Date: Monday, January 18, 2010 Sheet 7 of 91



Calpella Platform Design Guide Revision 1.6

Page 89

2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX# [7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

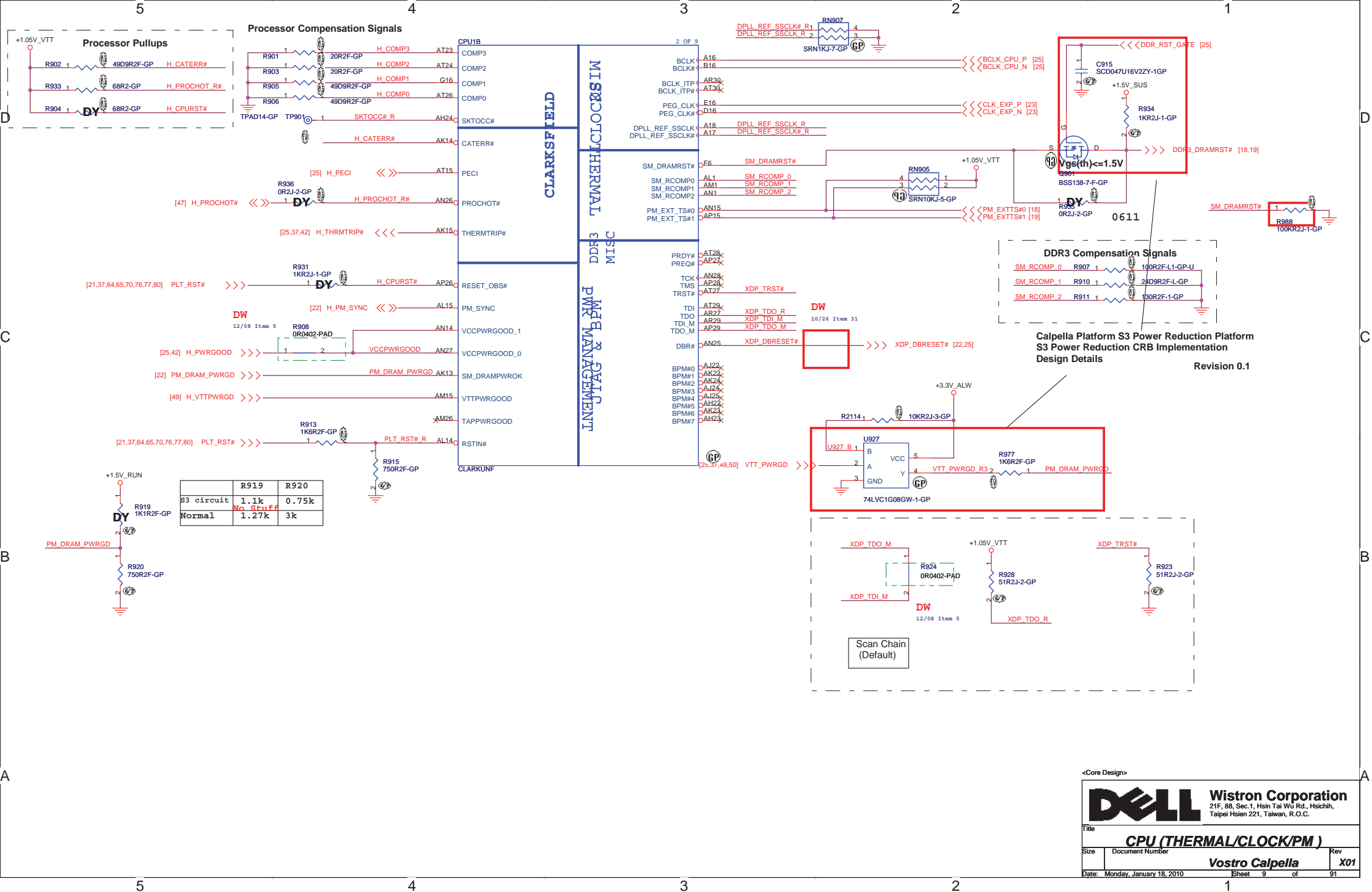


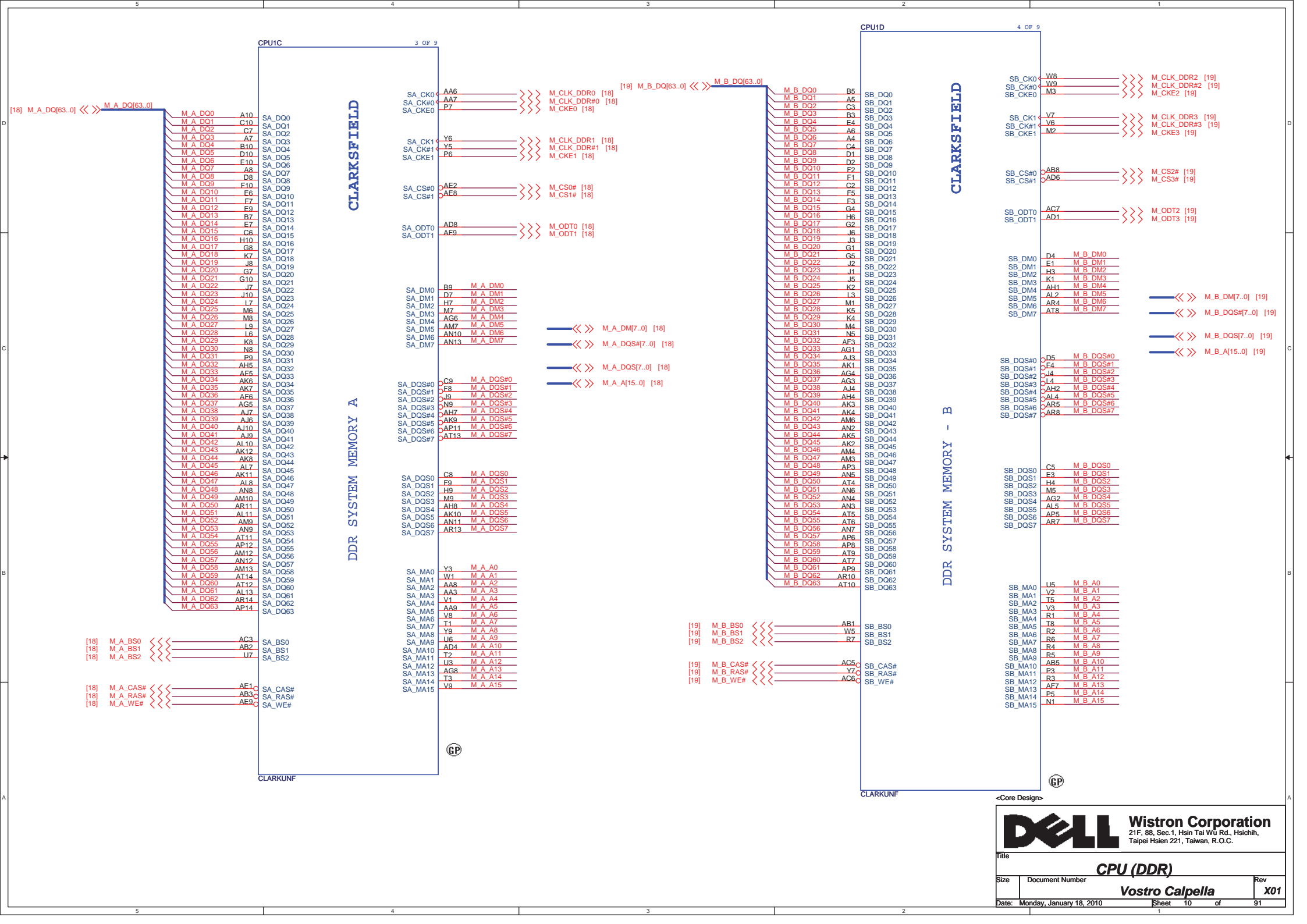
Reversal

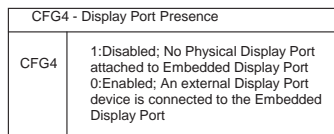
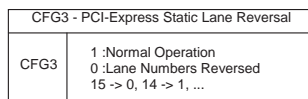
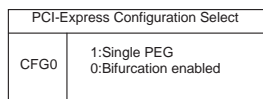
1. PCI-Express Static Lane Reversal (15 -> 0, 14 -> 1, ...)

<Core Design>

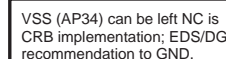
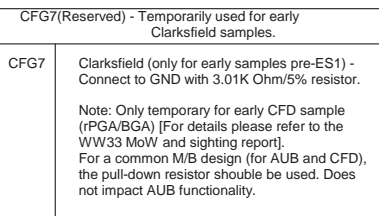
DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CPU (PCIe/DMI/FDI)			
Size	Document Number	Rev	
	Vostro Calpella		X01
Date: Monday, January 18, 2010	Sheet 8	of	91

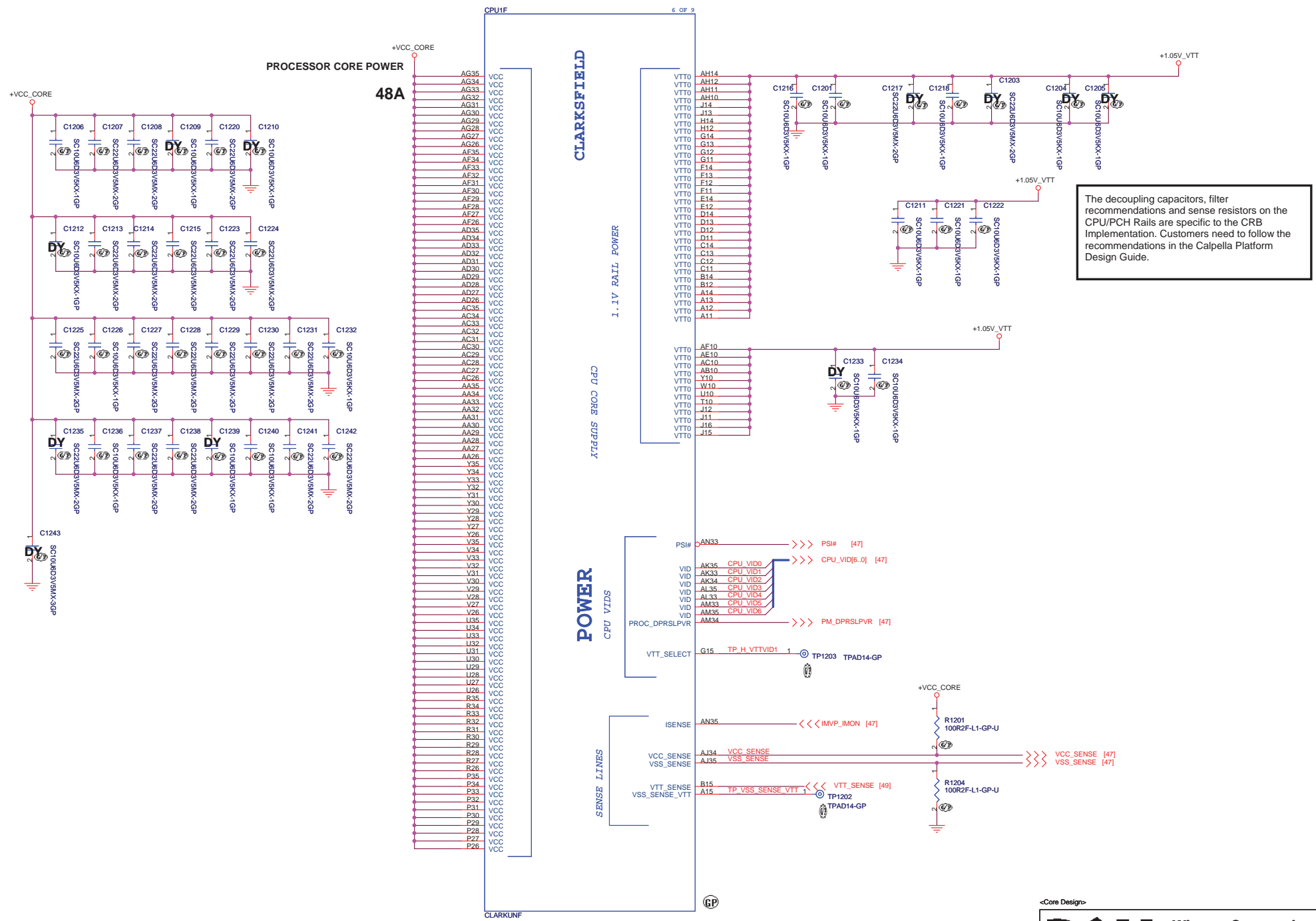







eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the `DDPD_CTRLDATA` strap high to 3.3V Core rail through 2.2 k Ω \pm 5% resistor, `LVDS (L_DDC_DATA)` strap as no connect and the eDP strap `CFG[4]` as no connect.



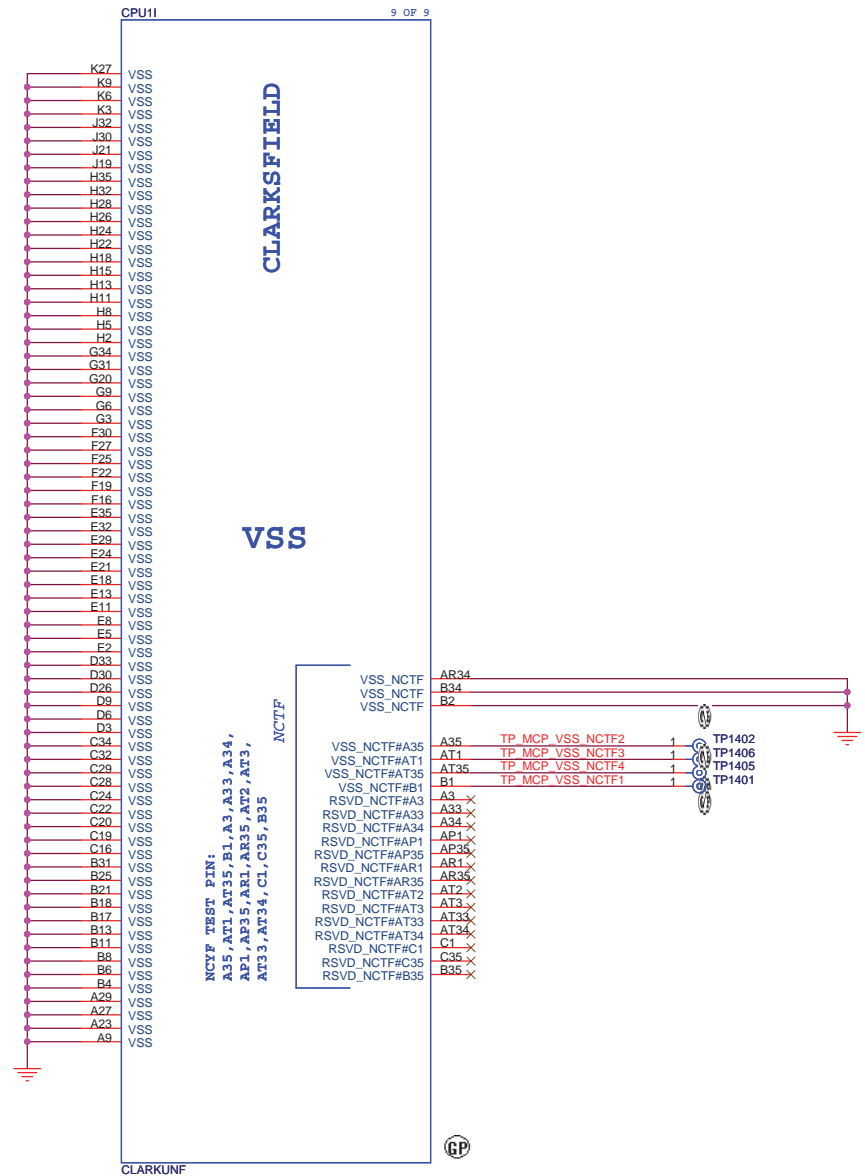
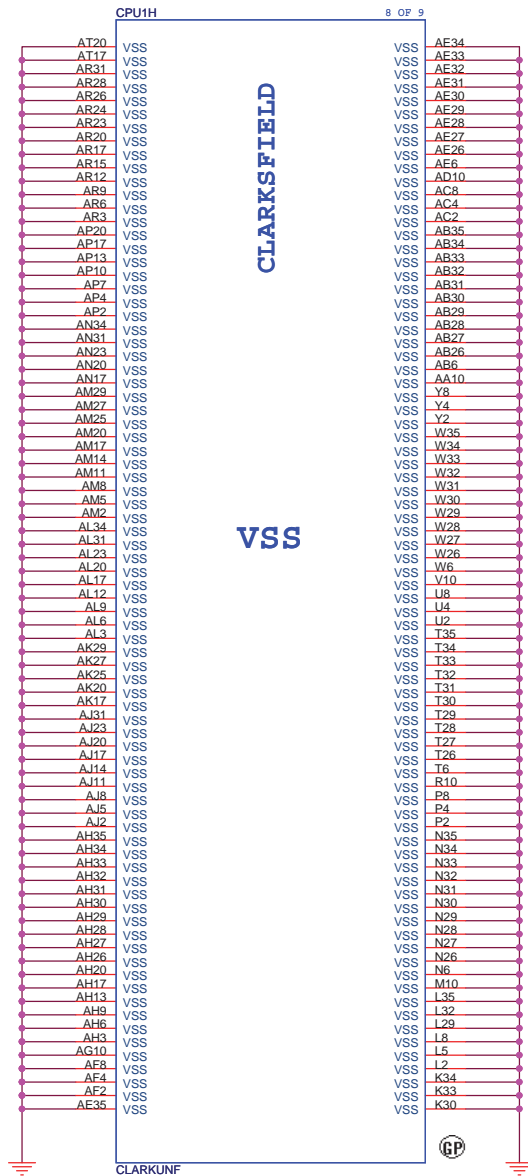


<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title CPU (VCC_CORE)		
Size	Document Number	Rev X01
Date: Monday, January 18, 2010	Sheet 12 of 91	



<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)


Size Document Number Rev

Vostro Calpella **X01**

Date: Monday, January 18, 2010 Sheet 14 of 91

(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size A3	Document Number	Rev X01
------------	-----------------	------------

Date: Monday, January 18, 2010	Sheet 15 of 91
--------------------------------	----------------

(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


Reserved

Size A3	Document Number	Rev X01
------------	-----------------	-------------------

Date: Monday, January 18, 2010	Sheet 16 of 91
--------------------------------	----------------

(Blank)

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

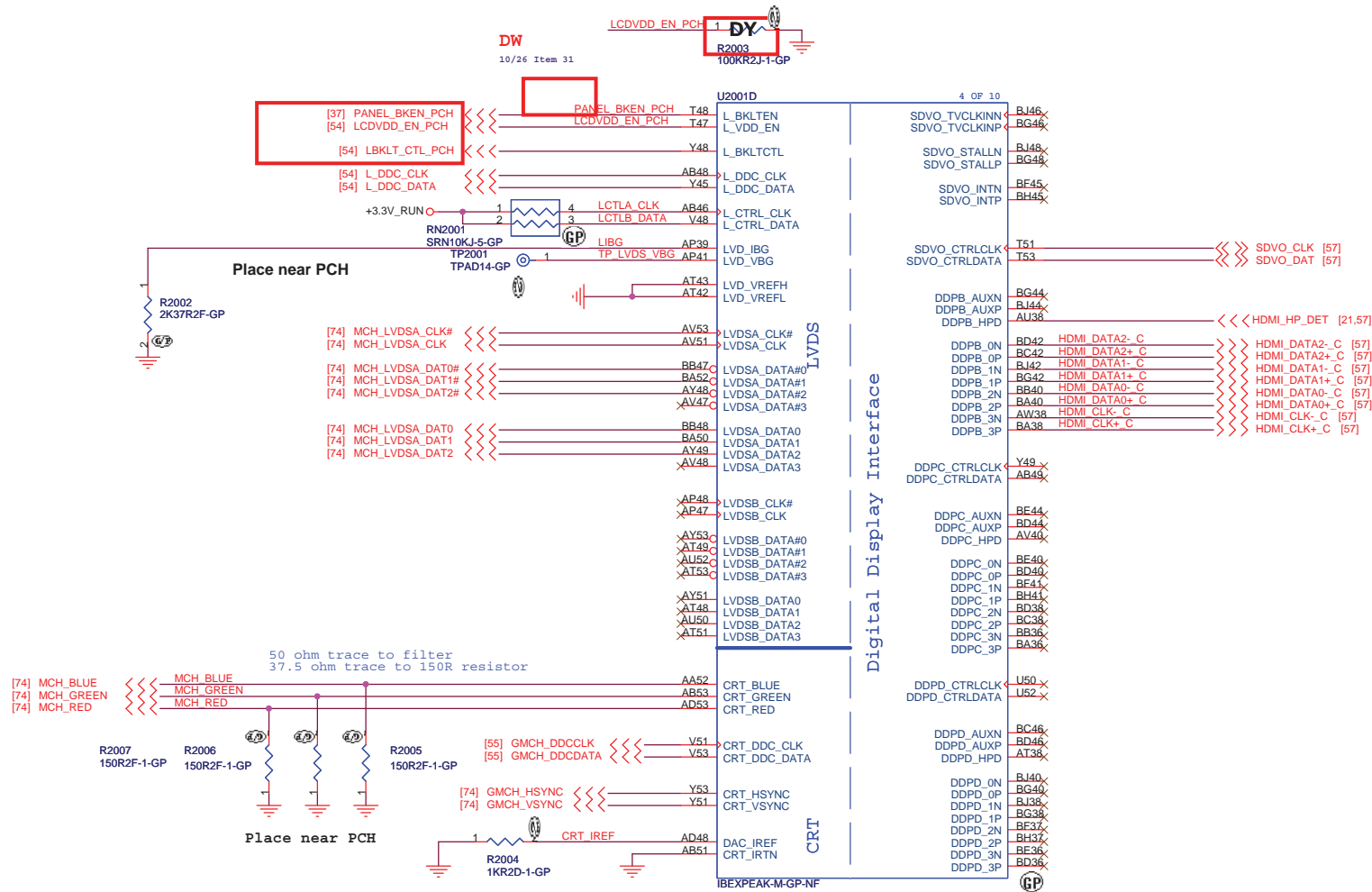
Title

(Reserve)

Size Custom	Document Number Vostro Calpella	Rev X01
----------------	---	-------------------

Date: Monday, January 18, 2010

Sheet 17 of 91

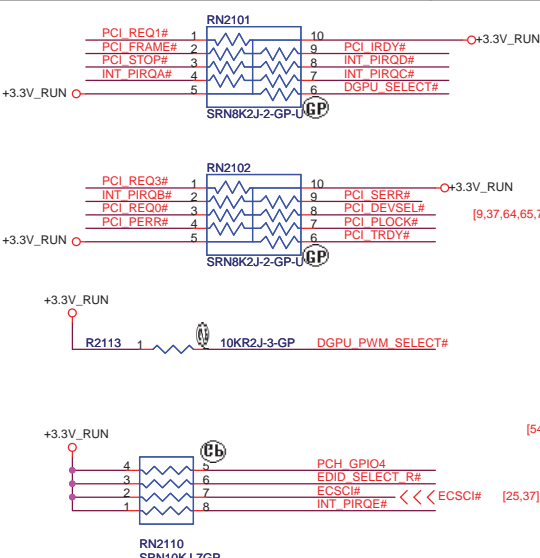


<Core Design>



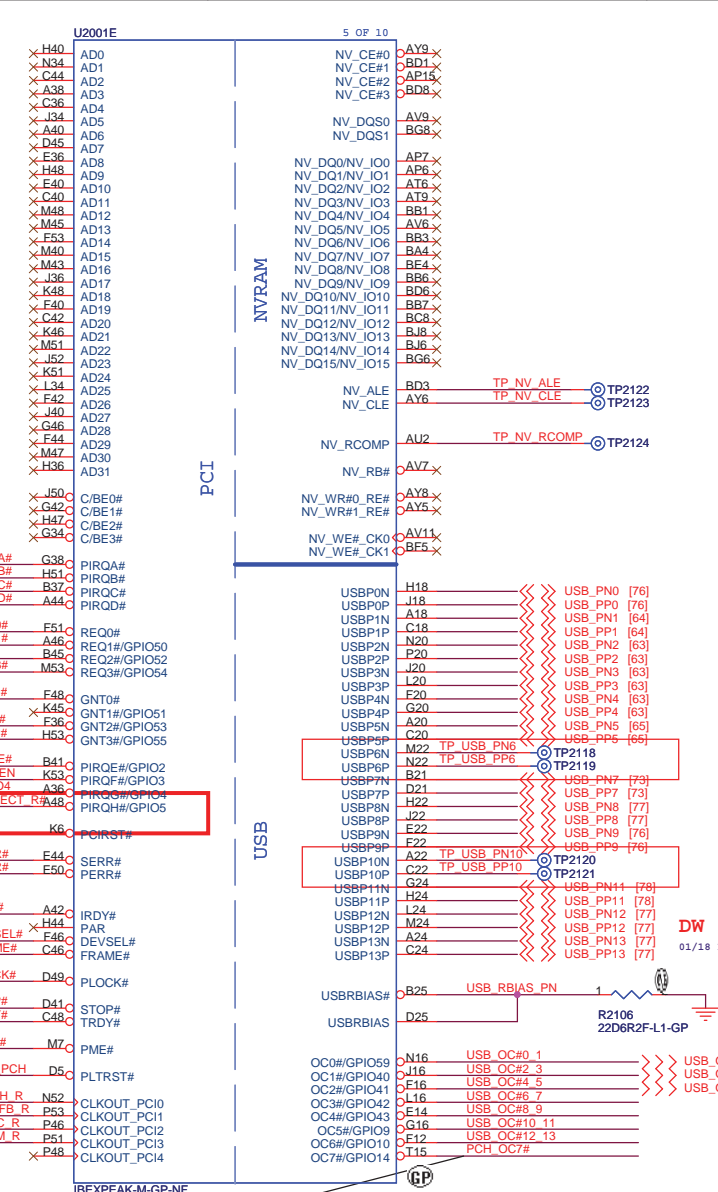
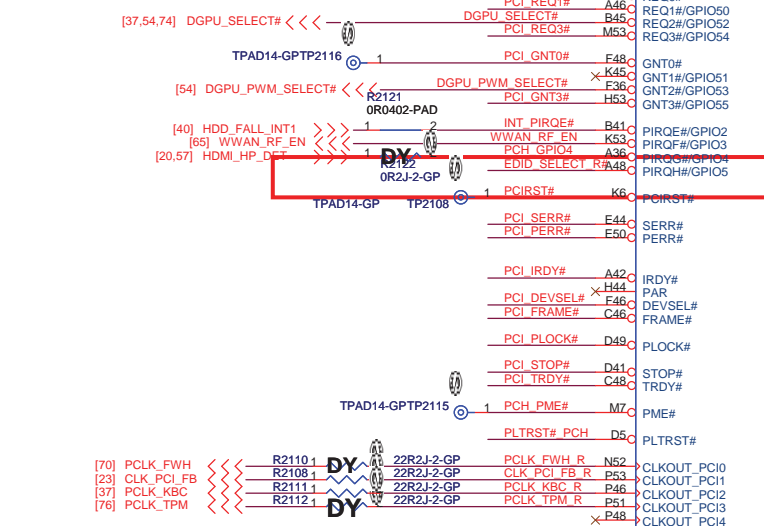
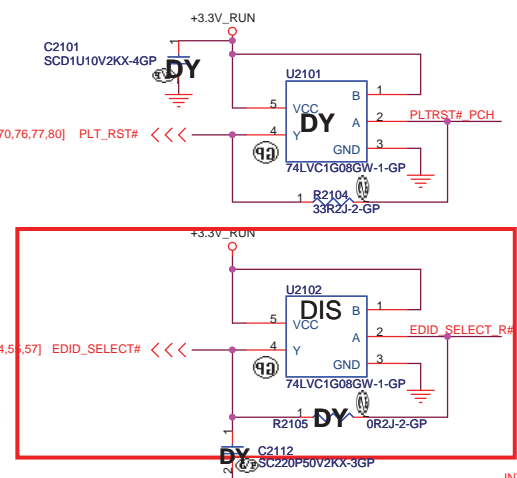
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (LVDS/CRT/DDI)			
Size	Document Number		Rev
	Vostro Calpella		X01
Date:	Monday, January 18, 2010		Sheet 20 of 91



DW
10/19 Changed
1.Changed EDID_SELECT# pin from PCH_GPIO66 to PCH_GPIO5 for fixed glitch

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

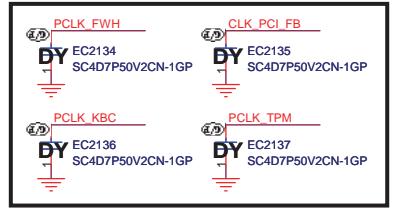


USB	
Pair	Device
0	USB1
1	WLAN
2	USB2
3	USB3
4	USB for ESATA
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Touch Panel
10	CAMERA
11	Biometric
12	New Card
13	CardReader

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



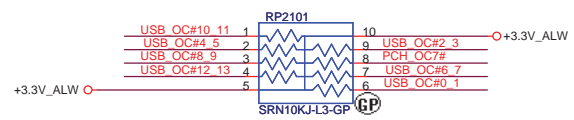
Reserve by pass cap near the U2001, For EMI



Calpella Platform Design Guide Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

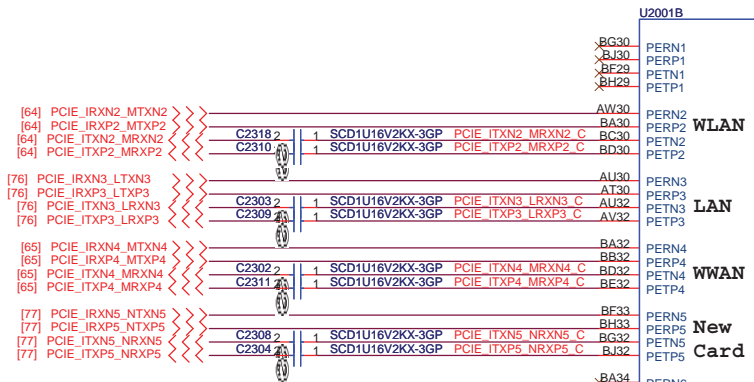
File: **PCH (PCI/USB/NVRAM)**

Size: Document Number

Date: Monday, January 18, 2010

Rev: **X01**

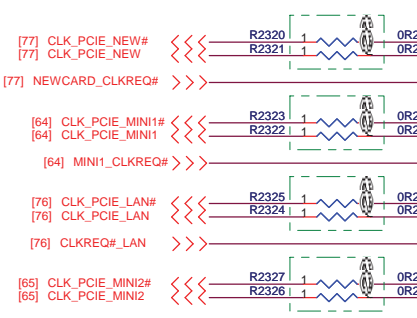
Sheet 21 of 91



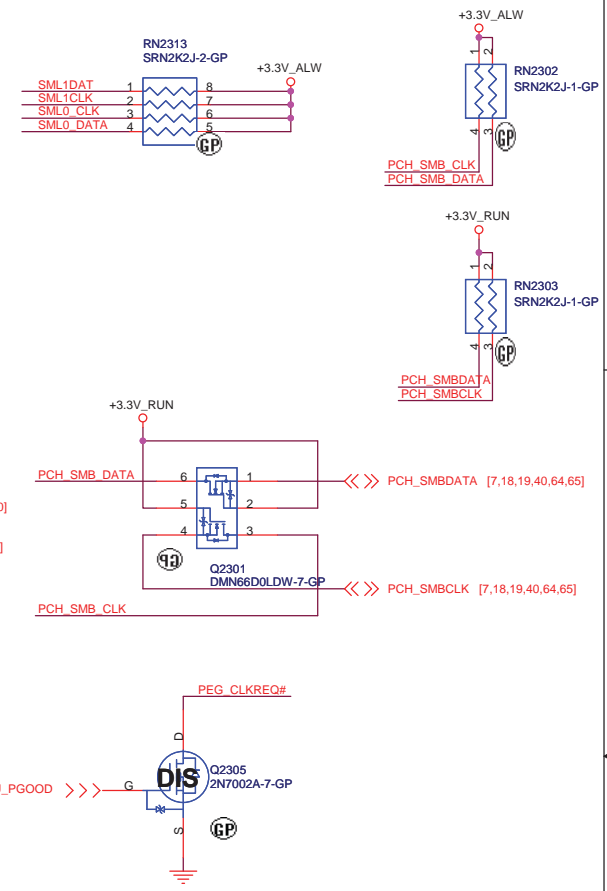
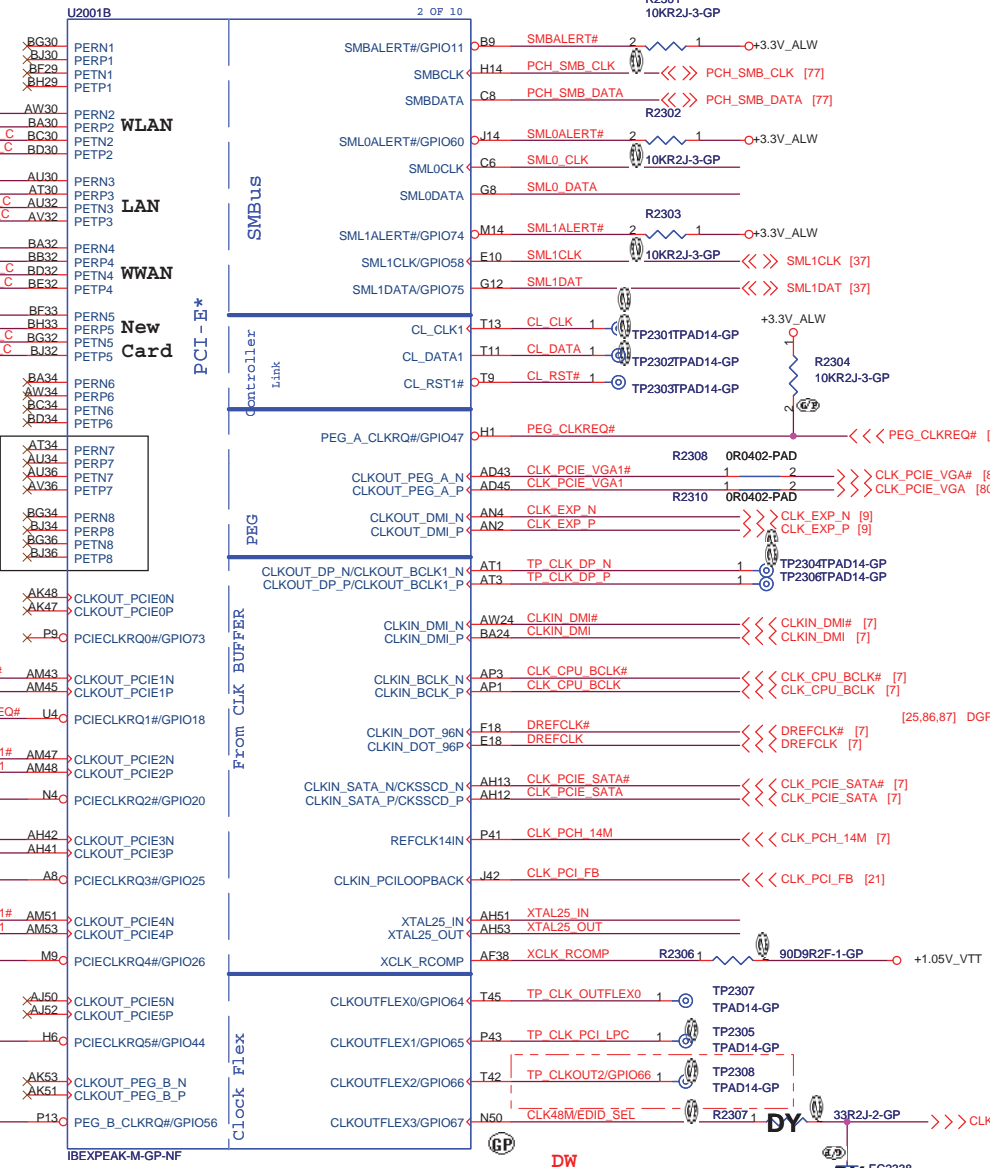
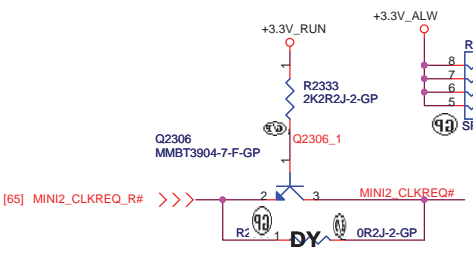
(Not available for HM55)

(Not available for HM55)

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN



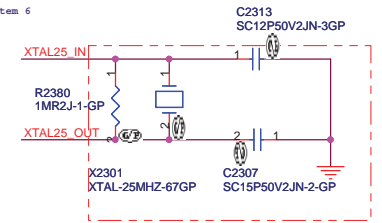
DW
12/10 Item 3
Reserve 0402 00hm resistors
, For RF Team to try solve PCIE noise



Display Clock Integration

	C2313	C2307	X2301	R2380
Normal	0R2J-2-GP	DY	DY	DY
dale DCI	SC18P	SC18P	25MHZ	1MR

DW
10/15 Item 6



<Core Design>

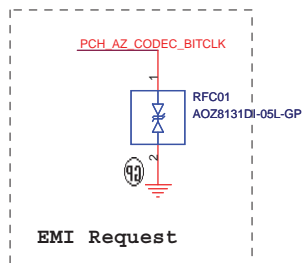
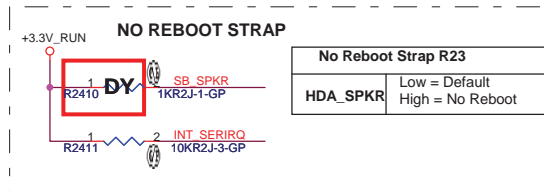
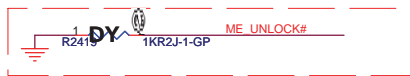
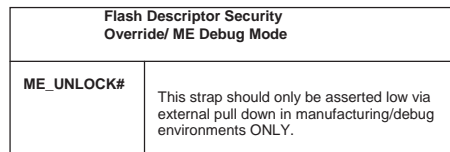
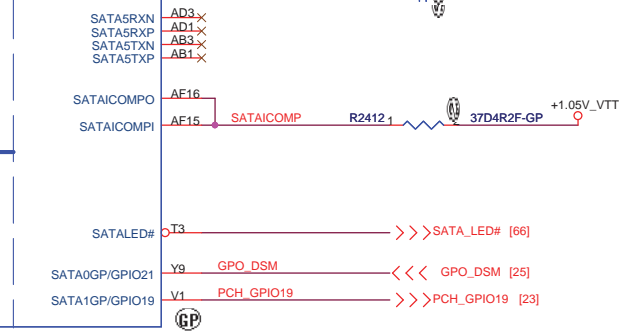
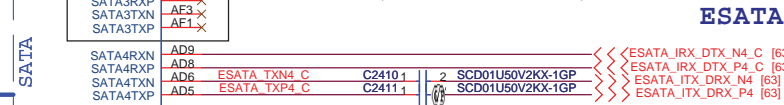
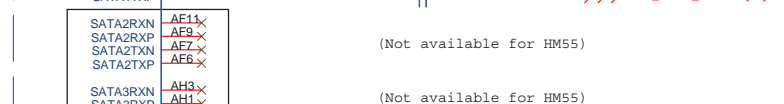
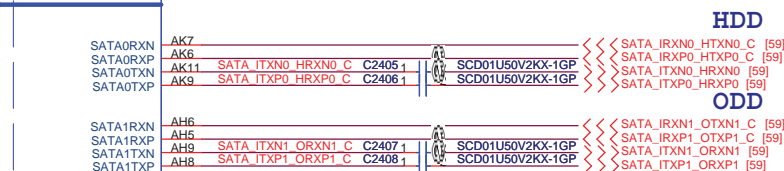
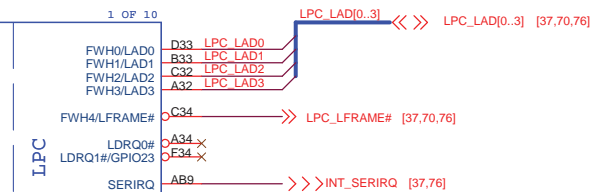
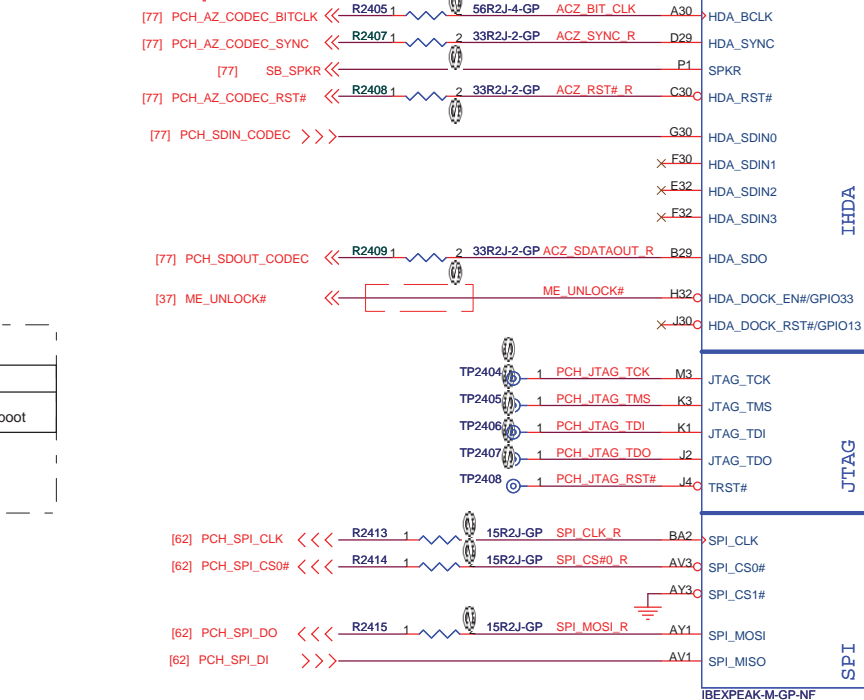
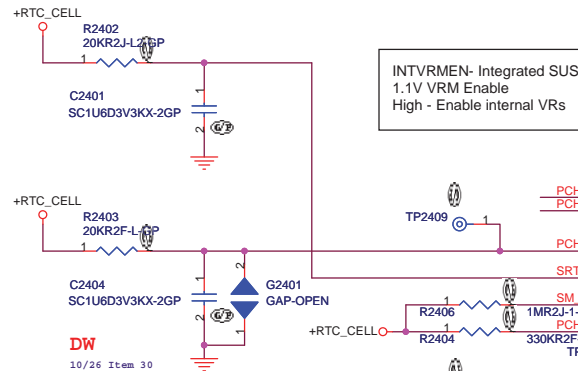
**Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

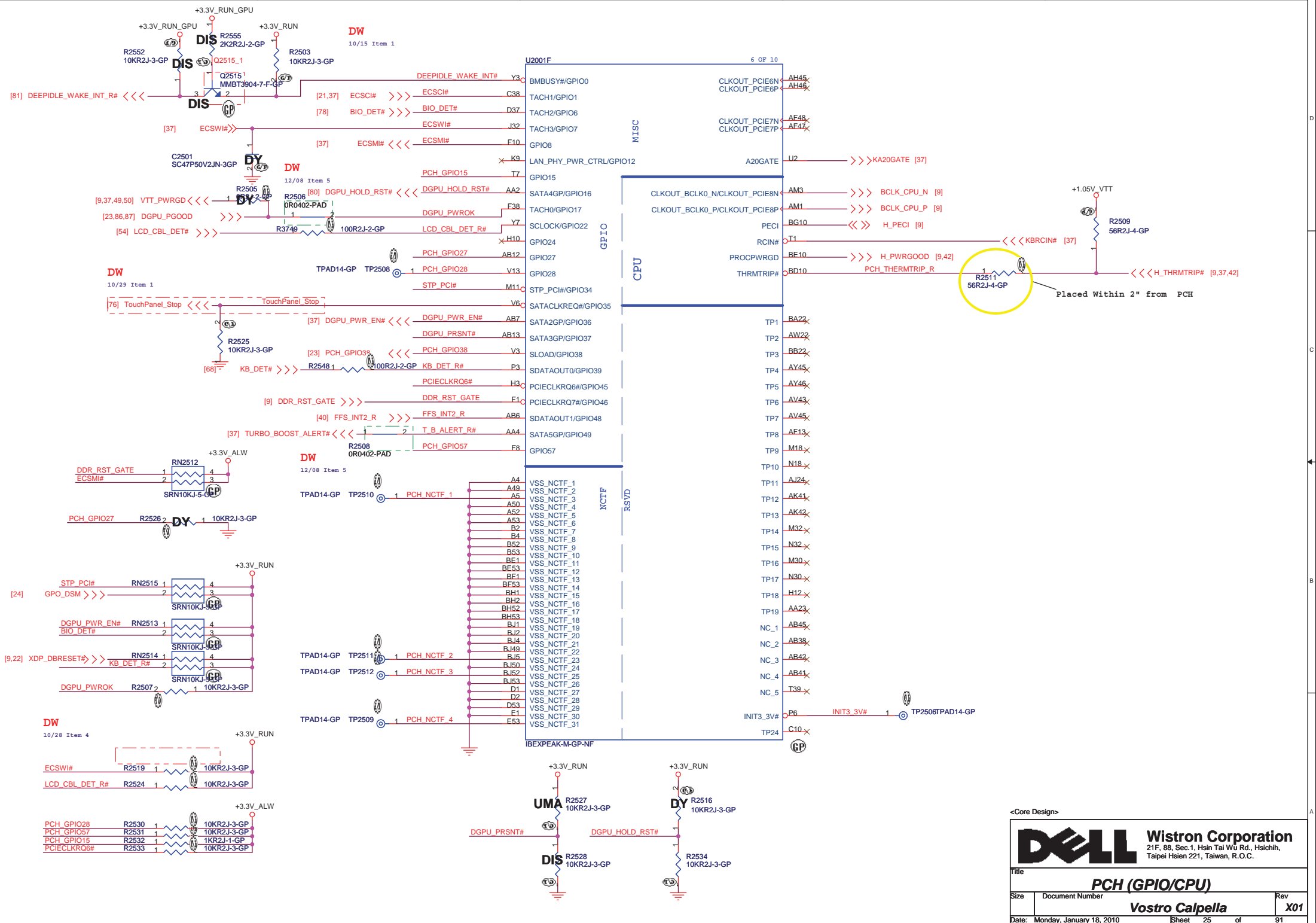
PCH (PCI-E/SMBUS/CLOCK/CL)

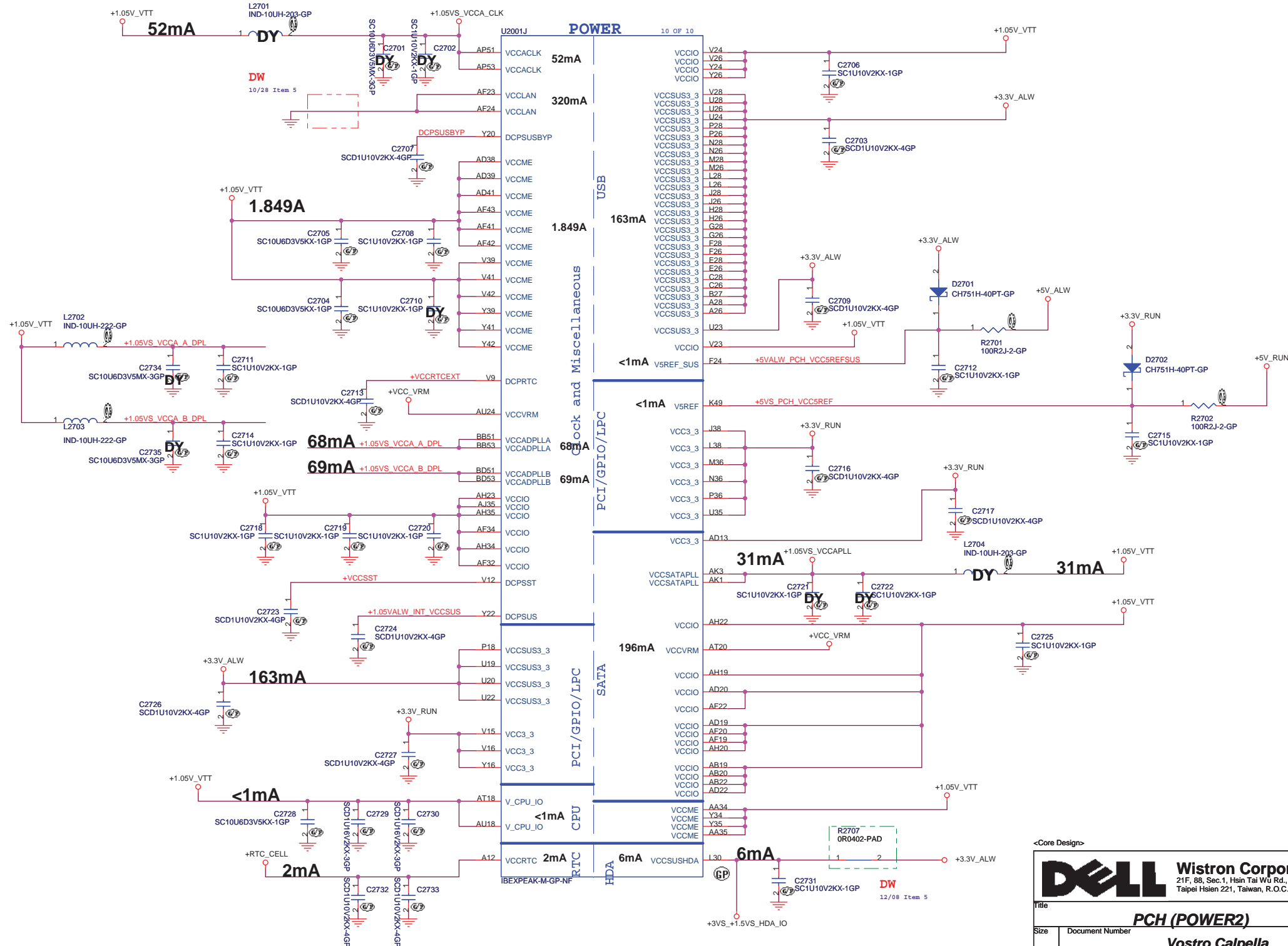
Vostro Calpella

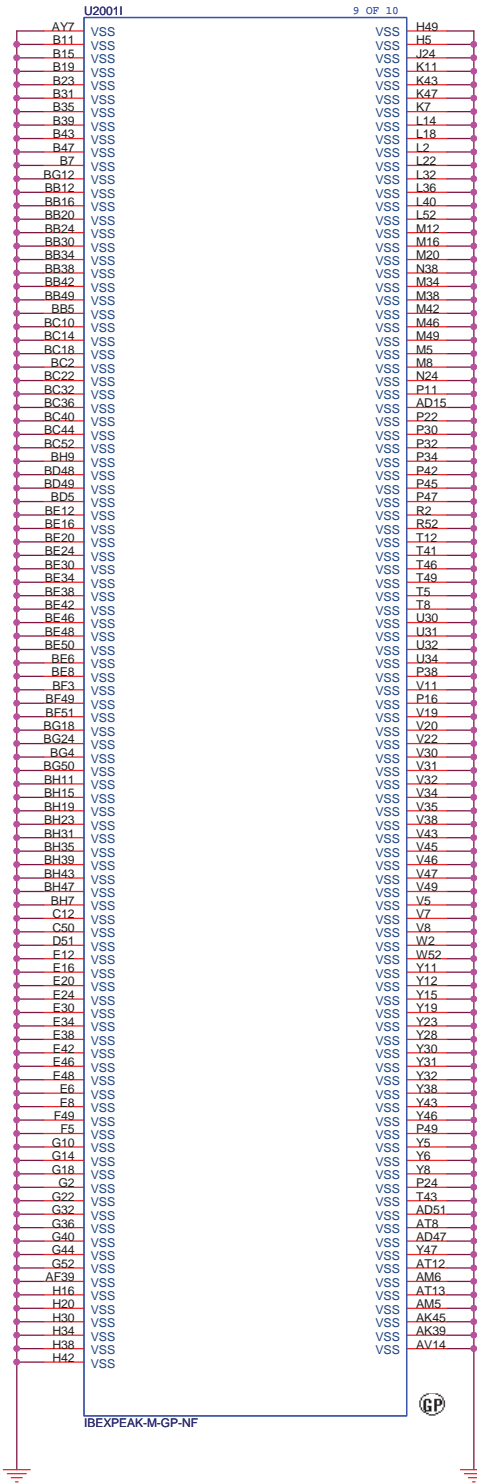
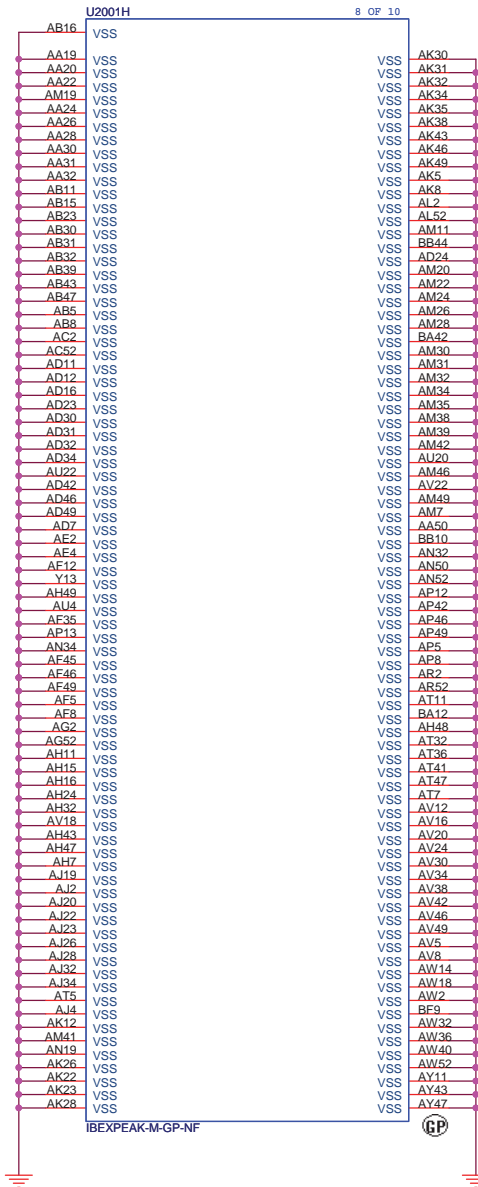
Rev **X01**

Sheet 23 of 91










(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size
Custom

Document Number
Vostro Calpella

Rev
X01

Date: Monday, January 18, 2010


Sheet 29 of 91

1

(Blank)

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010	Sheet 31 of 91
--------------------------------	----------------

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size
A3


Document Number
Vostro Calpella

Rev
X01

Date: Monday, January 18, 2010Sheet 32 of 91

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size
Custom

Document Number
Vostro Calpella

Rev
X01

Date: Monday, January 18, 2010


Sheet 33 of 91

1

(Blank)

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


(Reserve)

Size A3	Document Number Vostro Calpella	Rev X01
------------	---	-------------------

Date: Monday, January 18, 2010	Sheet 35 of 91
--------------------------------	----------------

(Blank)

<Core Design>



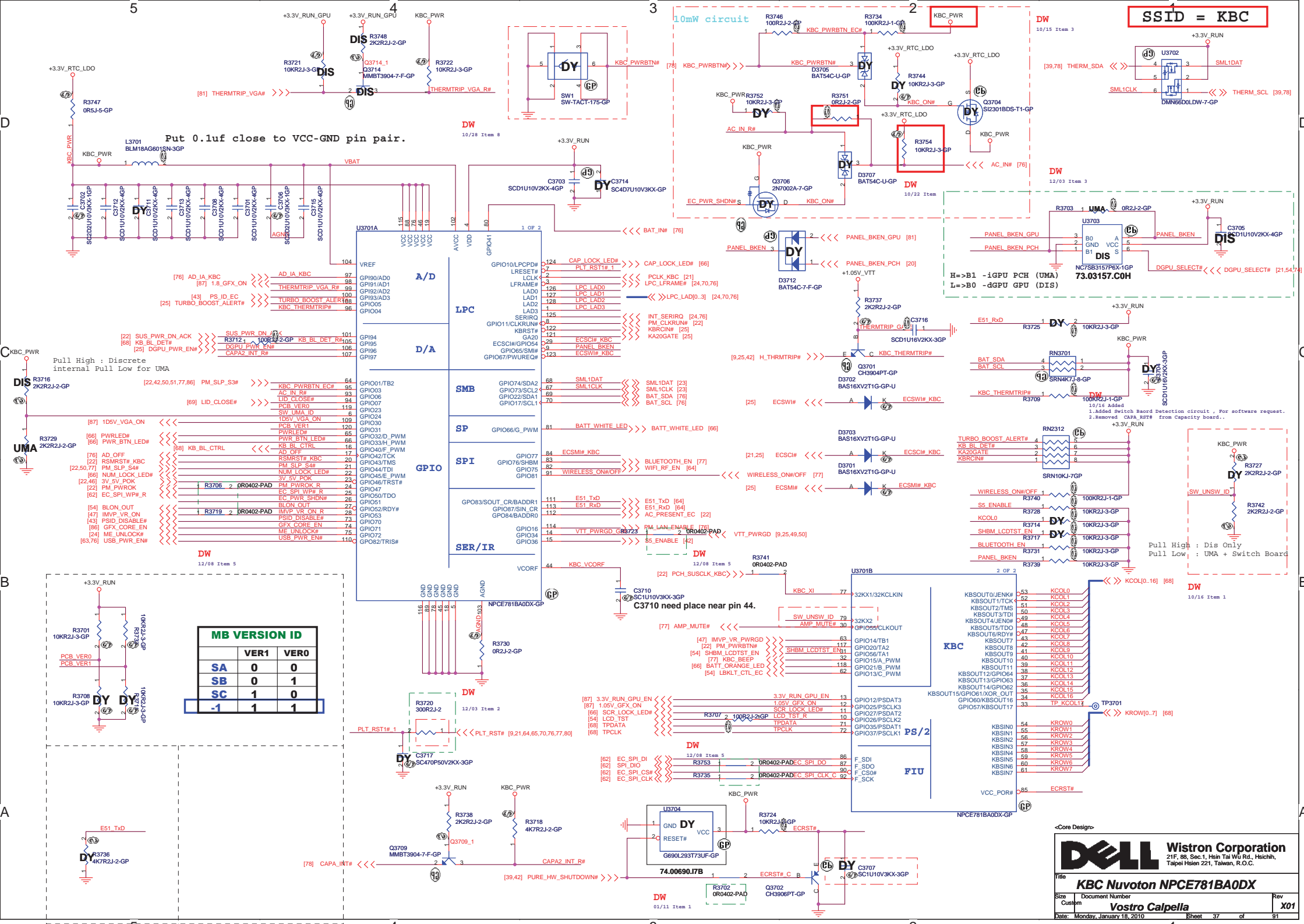
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

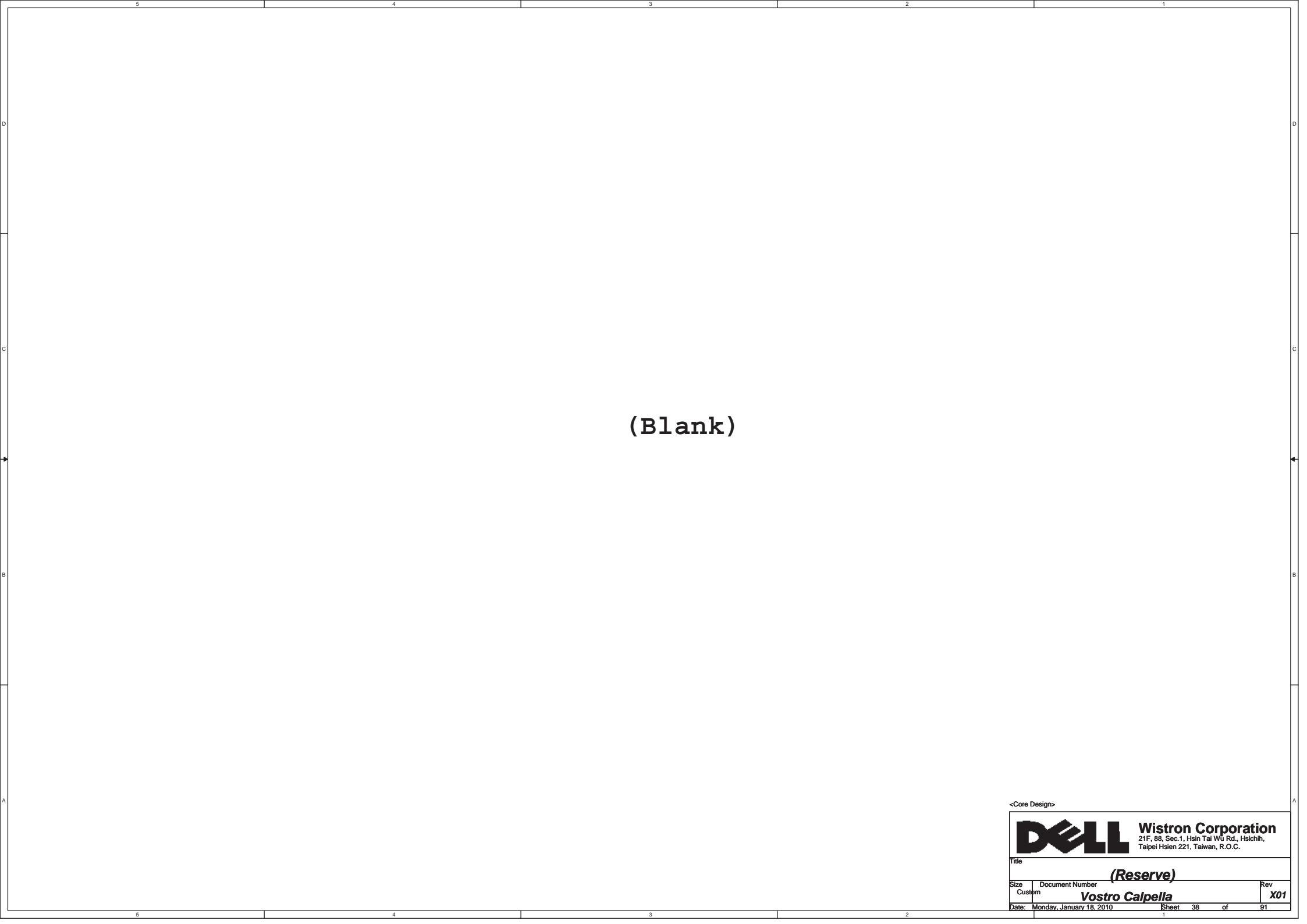
Title

(Reserve)

Size A3	Document Number Vostro Calpella	Rev X01
------------	---	-------------------


Date: Monday, January 18, 2010	Sheet 36 of 91
--------------------------------	----------------





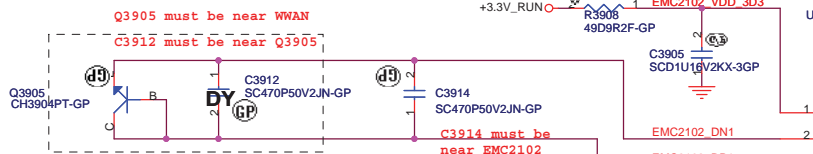
(Blank)

<Core Design>

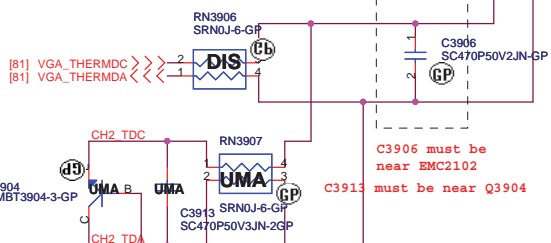
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserve)			
Size	Document Number		Rev
Custom	Vostro Calpella		X01
Date:	Monday, January 18, 2010		Sheet 38 of 91

SSID = Thermal

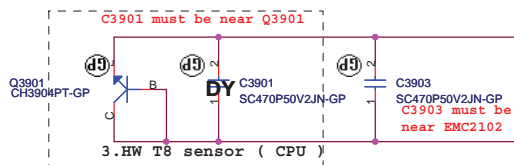
1. WWAN



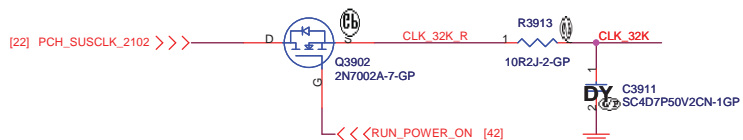
2. GPU Sensor



3. HW T8 sensor (CPU)

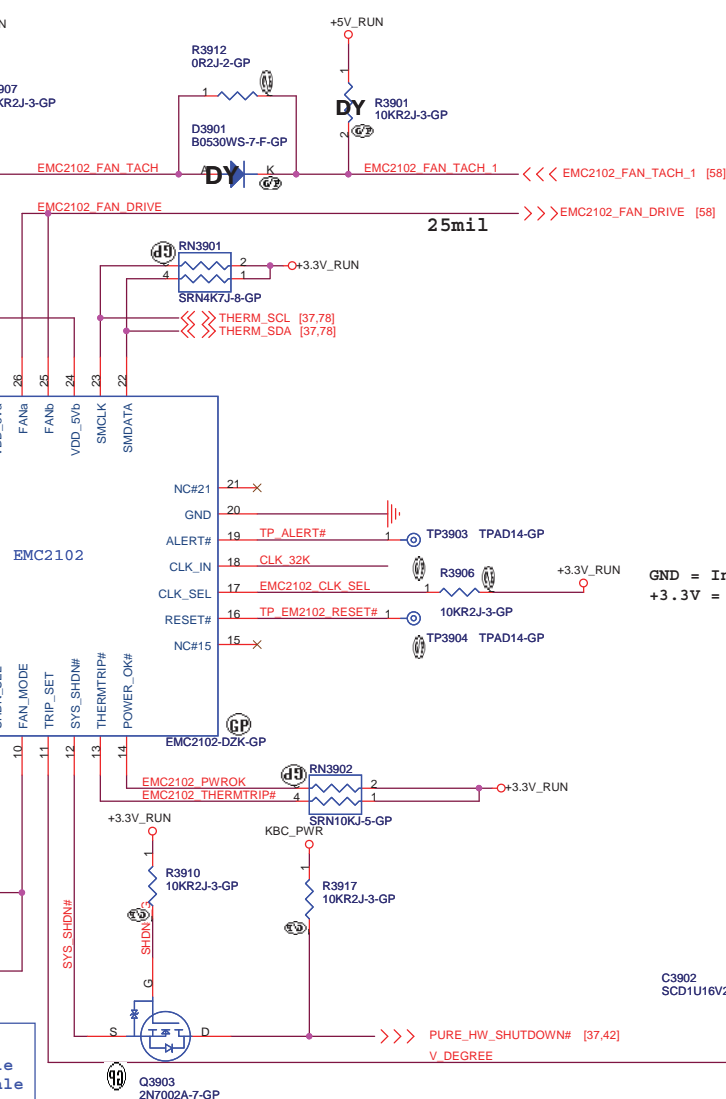


32K suspend clock output



GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale



GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

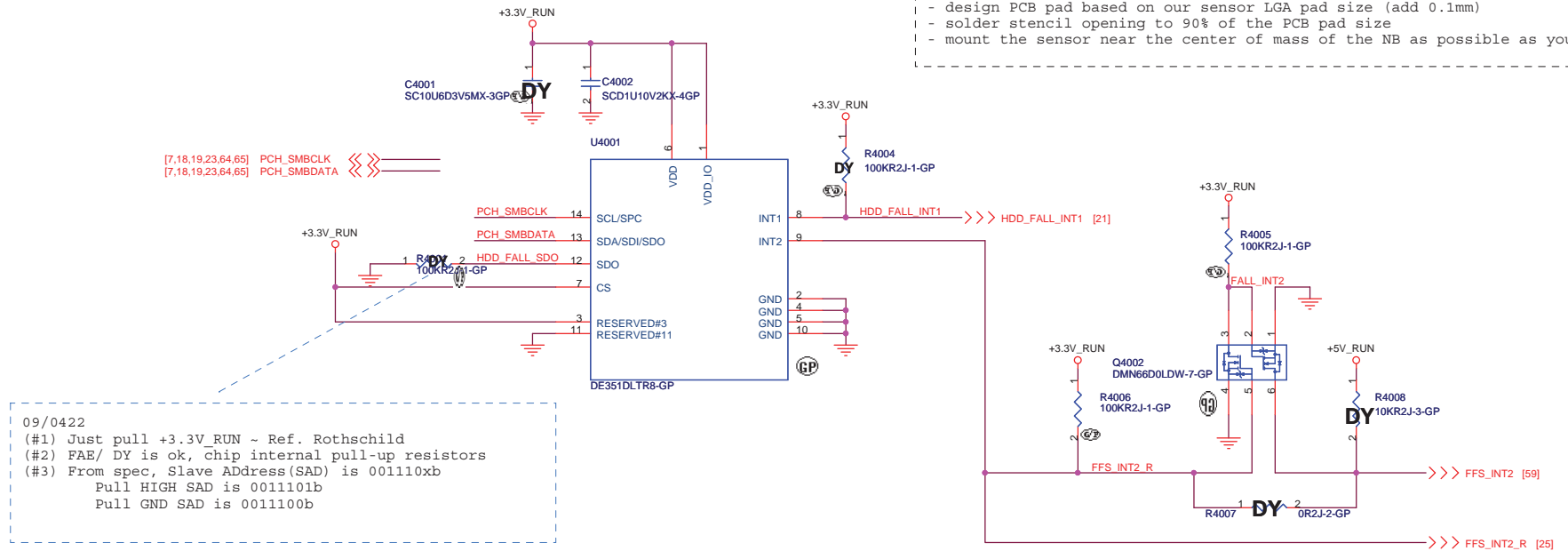
TRIP_SET Pin Voltage
 $V_DEGREE = (((Degree - 75) / 21))$
T8 shutdown is set 86 deg-C.

<Core Design>

SSID = User.Interface

Free Fall Sensor

- Note
- no via, trace, under the sensor (keep out area around 2mm)
 - stay away from the screw hole or metal shield soldering joints
 - design PCB pad based on our sensor LGA pad size (add 0.1mm)
 - solder stencil opening to 90% of the PCB pad size
 - mount the sensor near the center of mass of the NB as possible as you can




- Note
- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

<Core Design>

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010

Sheet 41 of 91

1

SSID = Reset.Suspend

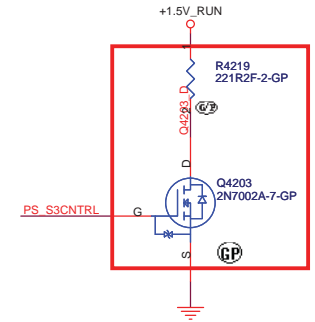
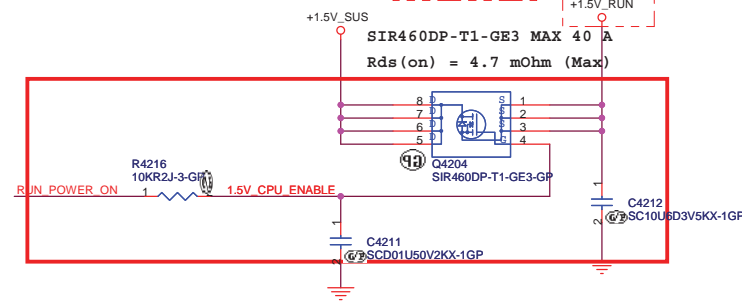
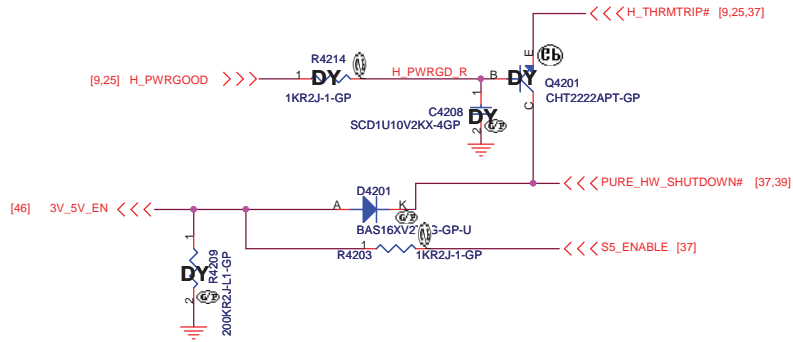
+1.5V_RUN:

Peak current: 4650 mA

Design current: 3255 mA

DW

10/26 Item 3



Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details

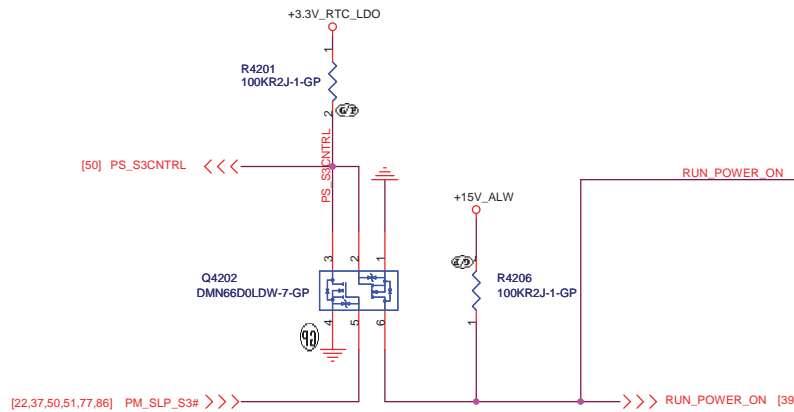
Revision 0.1

Peak current: 5605.6mA (HD:1100 ODD:2500)

Design current: 3923.92 mA

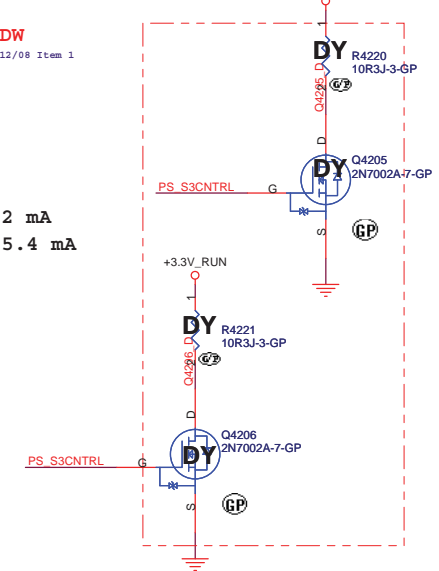
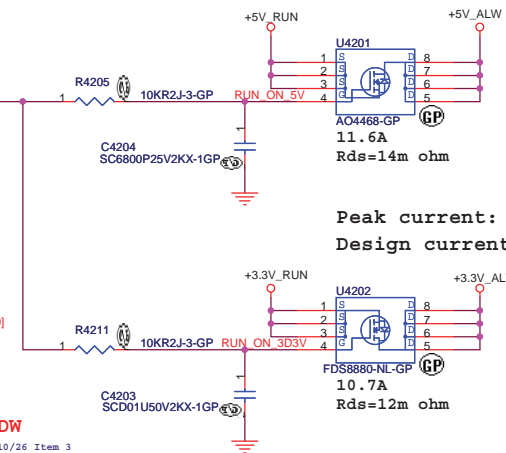
DW

12/08 Item 1

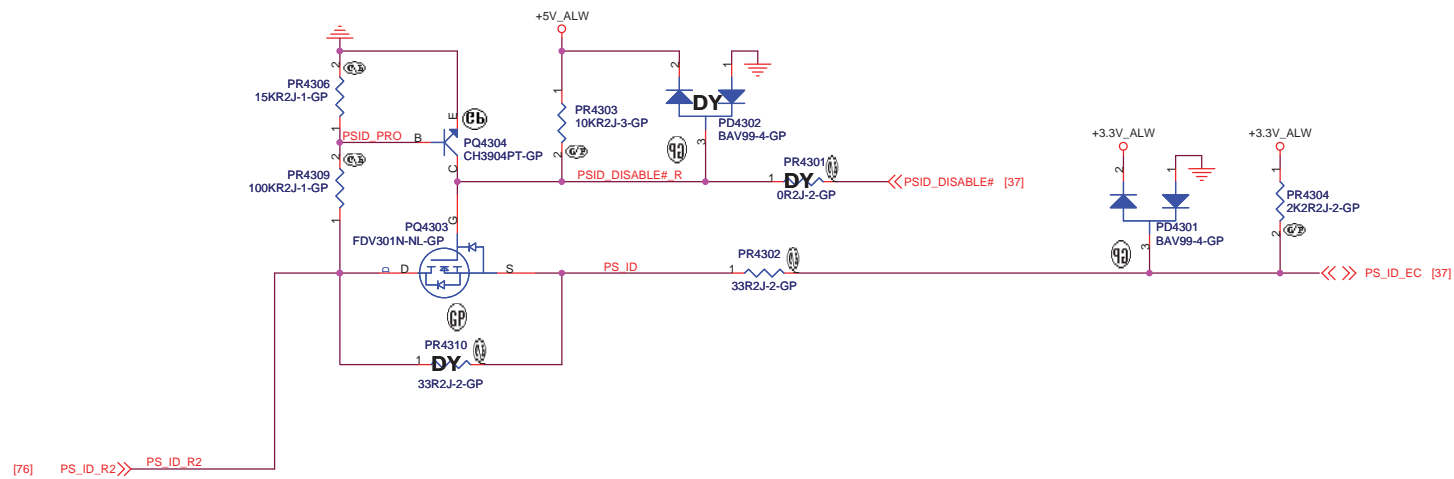


DW

10/26 Item 3




<Core Design>



<Core Design>

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

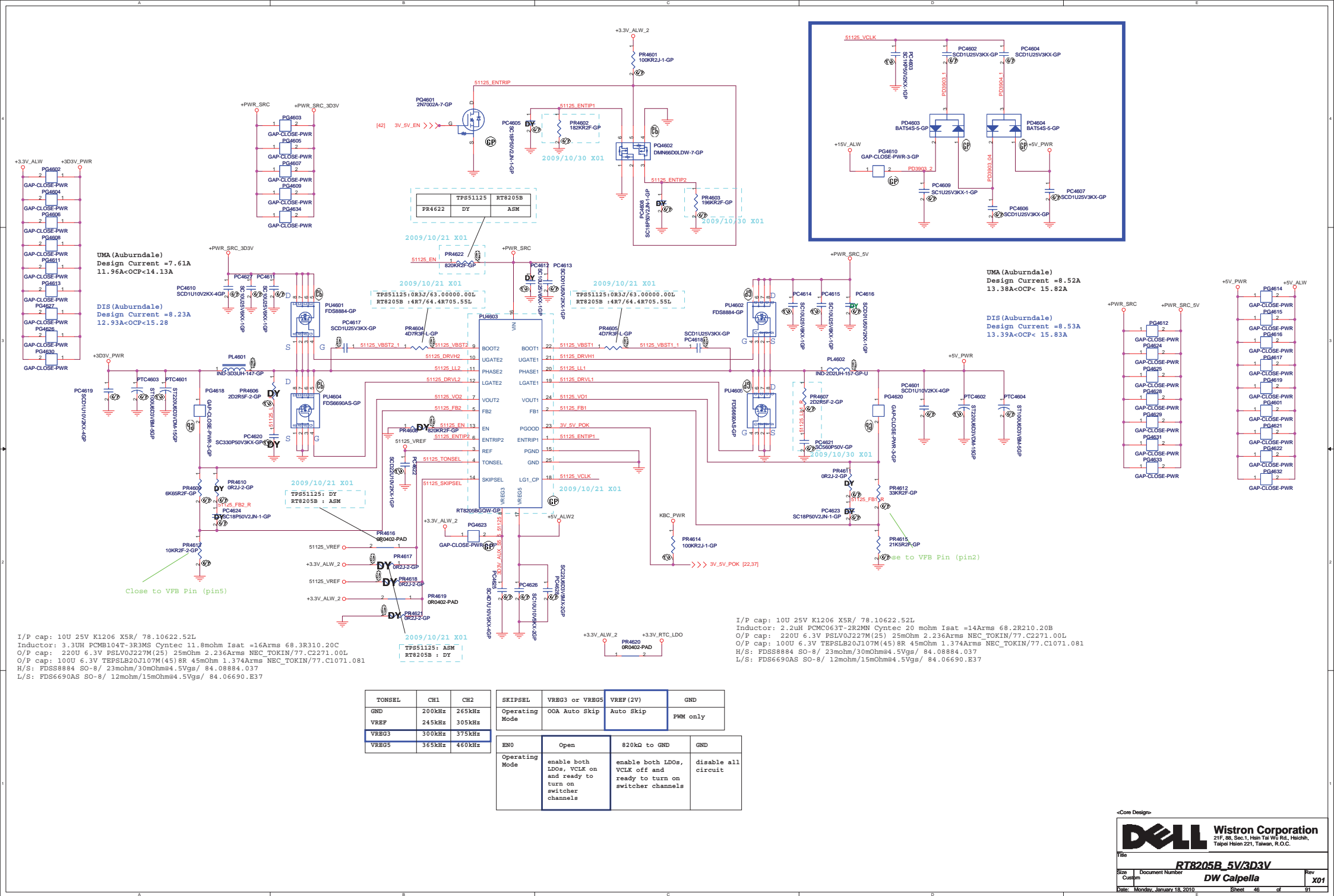
Title

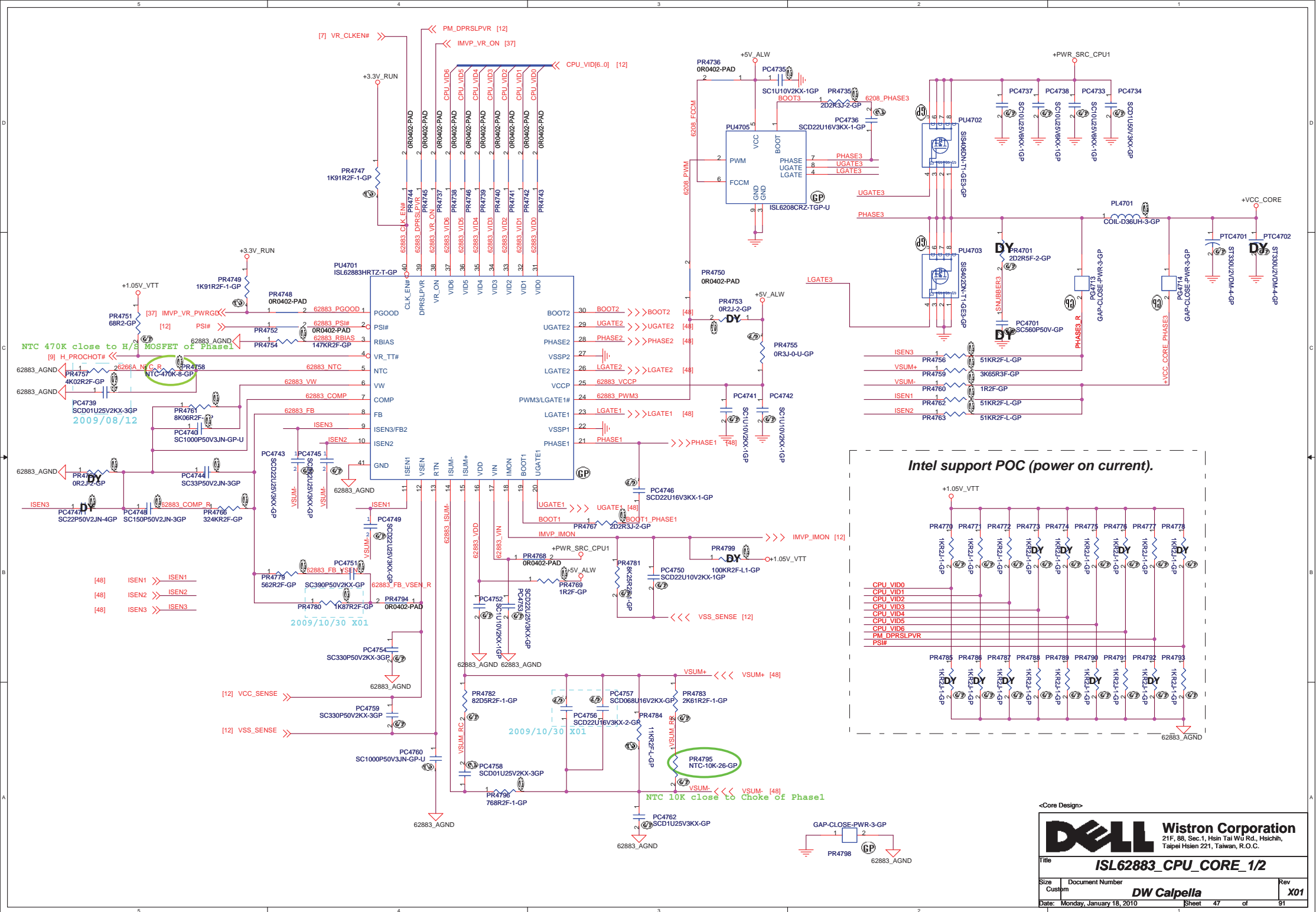
(Reserve)

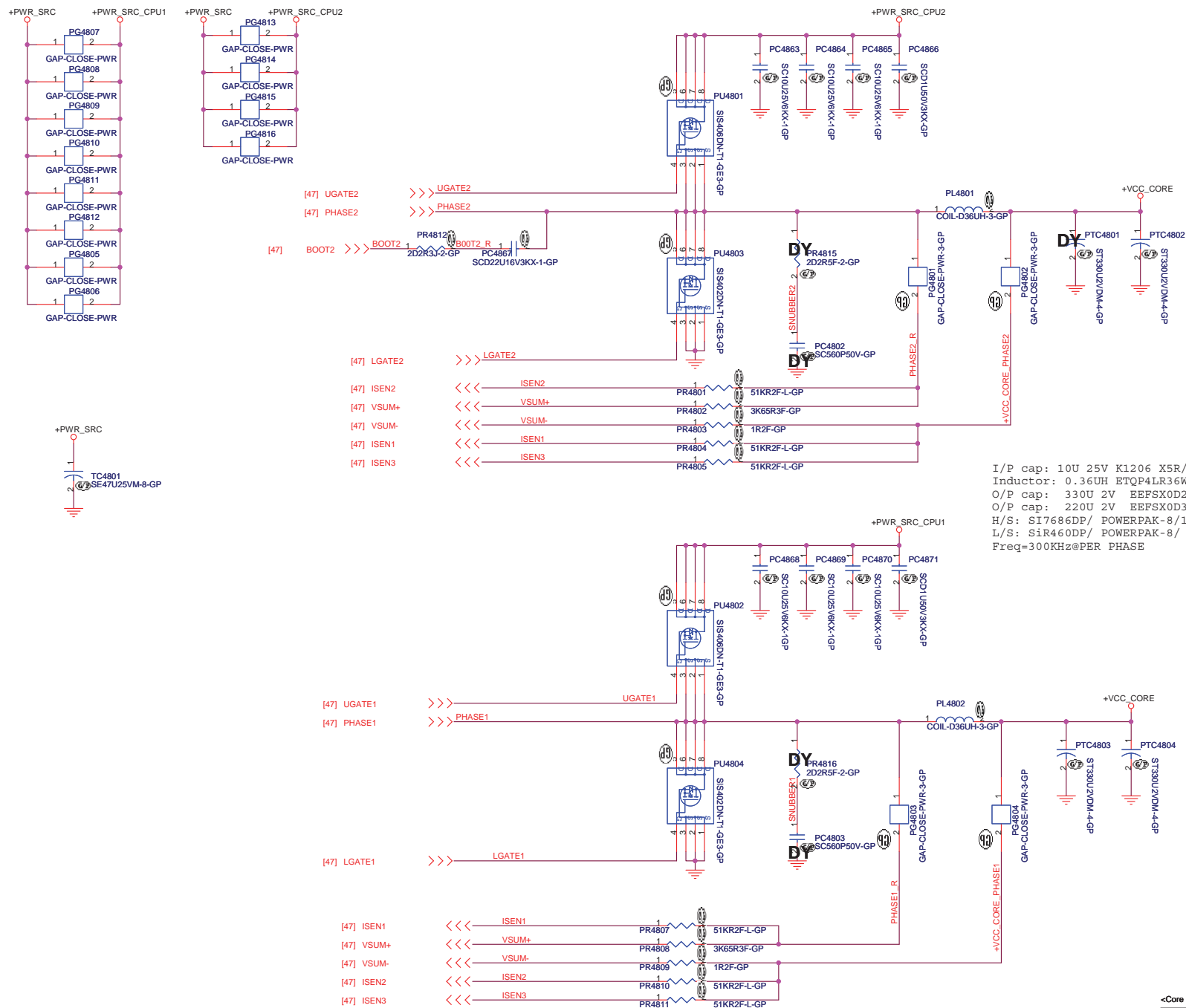
Size A3	Document Number Vostro Calpella	Rev X01
------------	---	-------------------

Date: Monday, January 18, 2010	Sheet 44 of 91
--------------------------------	----------------

(Blank)







DIS(Auburndale)
 Design Current = 34A
 Peak Current=48A
 57.6A<OCP< 67.2A

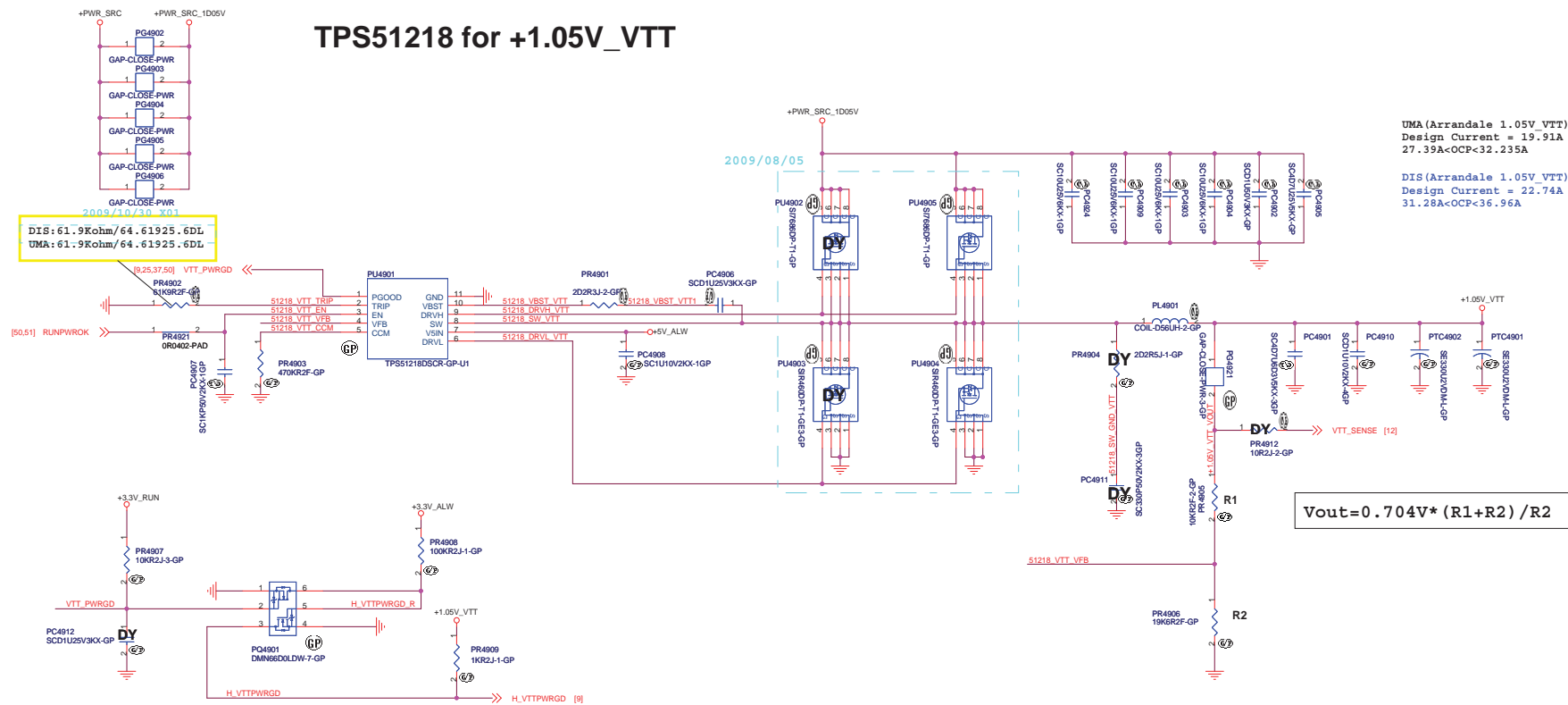
UMA(Auburndale)
 Design Current = 34A
 Peak Current=48A
 57.6A<OCP< 67.2A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
 O/P cap: 330U 2V BEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
 O/P cap: 220U 2V BEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
 H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
 Freq=300KHz@PER PHASE

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title ISL62883_CPU_CORE_2/2	
Size Custom	Document Number DW Calpella	Rev X01	
Date: Monday, January 18, 2010	Sheet 48 of 91		

TPS51218 for +1.05V_VTT



UMA(Arrandale 1.05V_VTT)
Design Current = 19.91A
27.39A<OCP<32.235A

DIS(Arrandale 1.05V_VTT)
Design Current = 22.74A
31.28A<OCP<36.96A

$$V_{out} = 0.704V * (R1 + R2) / R2$$

Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SIR474DP-T1-GE3/10mohm/ 12mOhm@4.5Vgs/ 84.00474.037
L/S: SI7170DP-T1-GE3/3.6mOhm/4.3mohm@4.5Vgs/ 84.07170.037

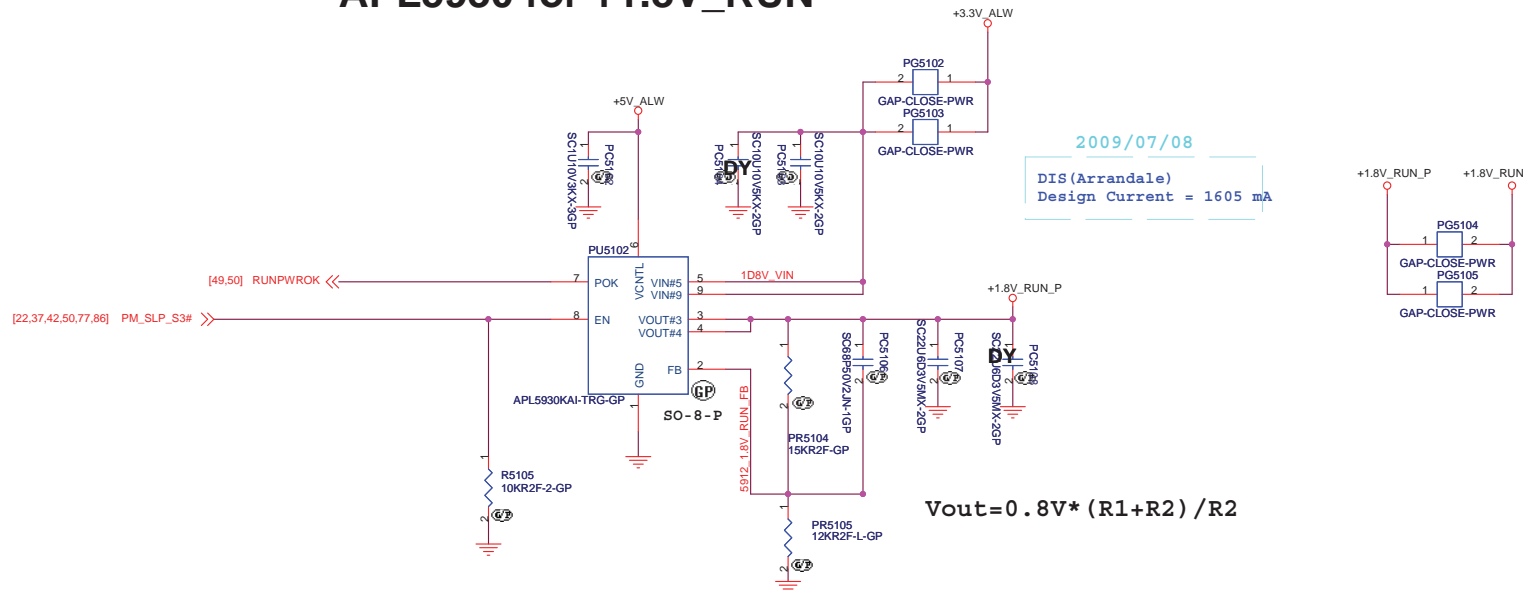
<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
TPS51218 +1.05V_VTT		
Size	Document Number	Rev
Custom	DW Calpella	X01
Date: Monday, January 18, 2010		
Sheet 49 of 91		

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN




<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title APL5930 +1.8V RUN			
Size Custom	Document Number DW Calpella	Rev X01	
Date: Monday, January 18, 2010	Sheet 51 of 91		

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

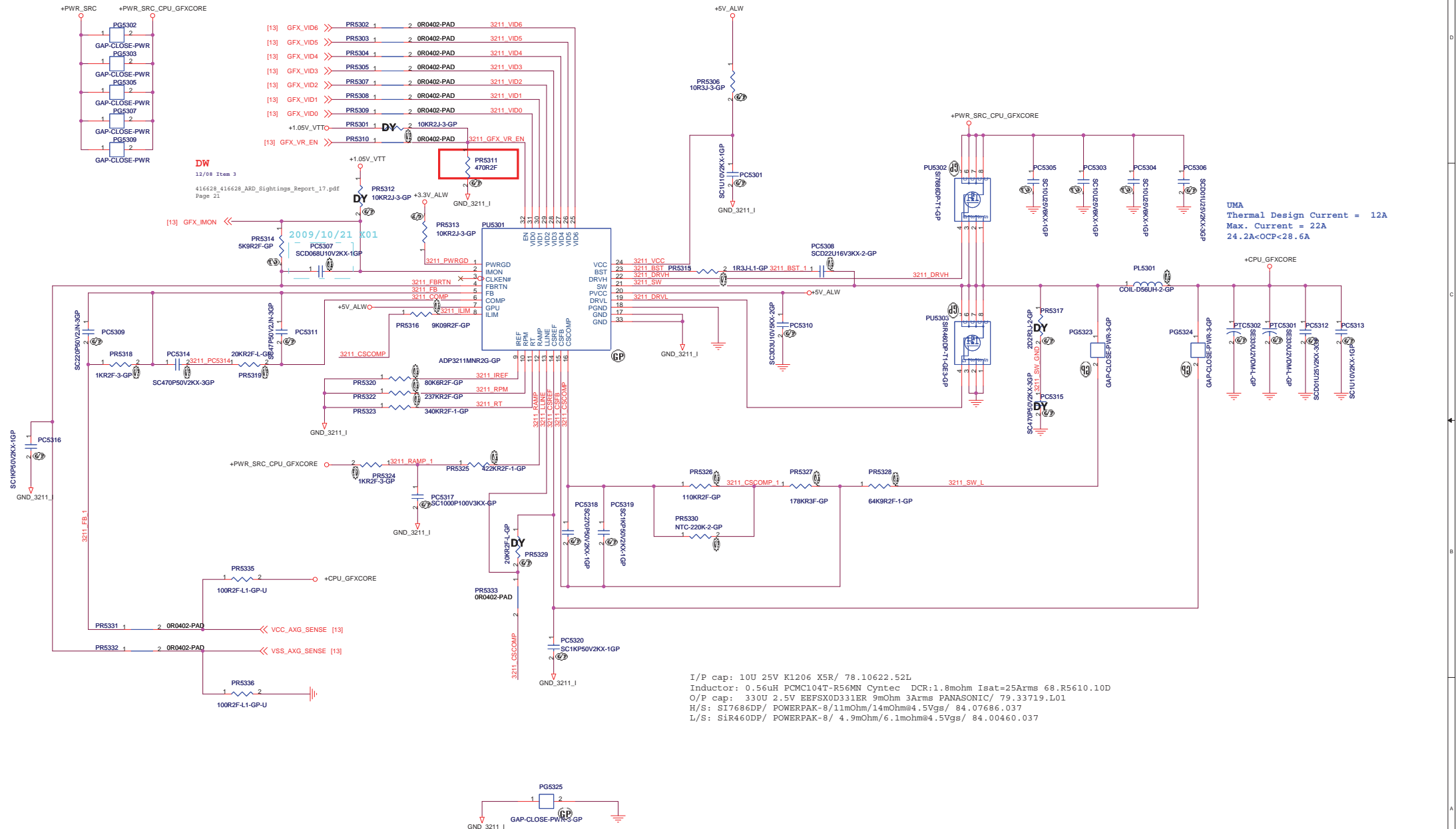
(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010

Sheet 52 of 91

SSID = CPU.GFX.Regulator



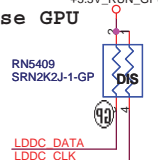
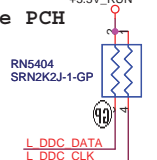
<Core Design>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
ADP3211 CPU GFXCORE			
Size			
DW Calpella UMA			
Rev			
X01			
Date:	Monday, January 18, 2010	Sheet	53 of 91

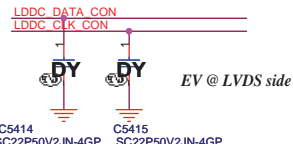
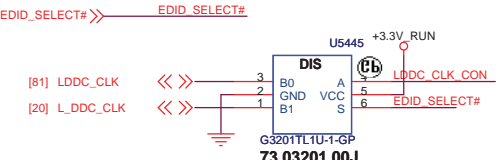
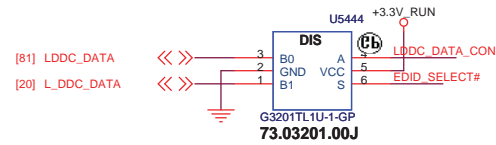
SSID = VIDEO

Close PCH

Close GPU

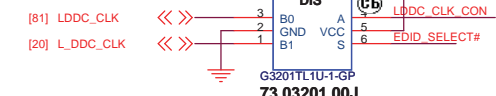


UMA/DIS LVDS DDC CLK/DAT select circuit



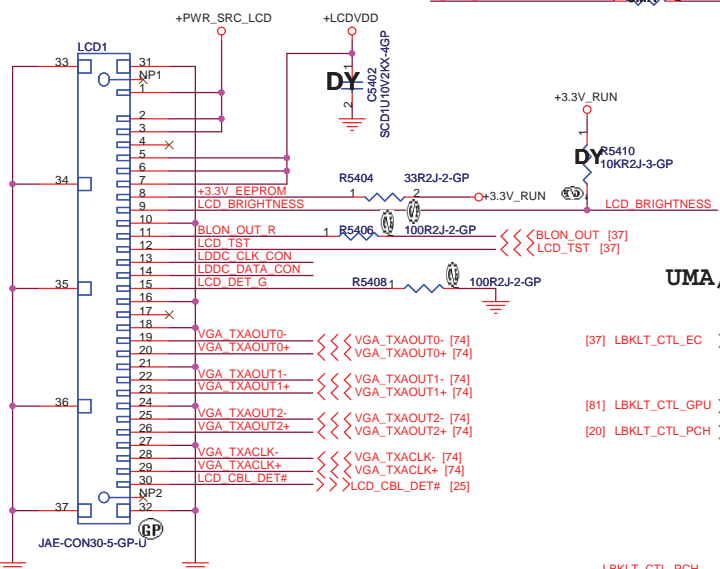
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

[21,55,57] EDID_SELECT# >>> EDID_SELECT#

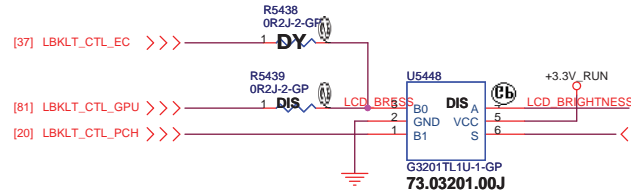


LDDC_DATA R5421 1 0R2J-2-GP LDDC_DATA_CON
LDDC_CLK R5420 1 0R2J-2-GP LDDC_CLK_CON

LVDS CONNECTOR

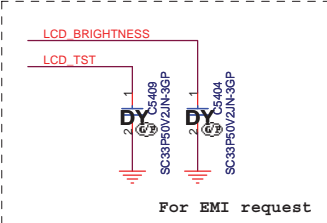


UMA/DIS LVDS PWM select circuit



H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

LBKLT_CTL_PCH R5422 1 0R2J-2-GP LCD_BRIGHTNESS
LBKLT_CTL_EC R5424 1 0R2J-2-GP LCD_BRIGHTNESS

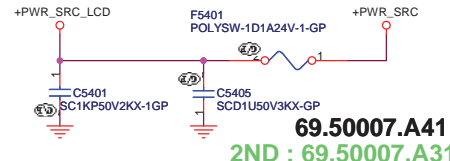


For EMI request

20.F1555.030

SSID = Inverter

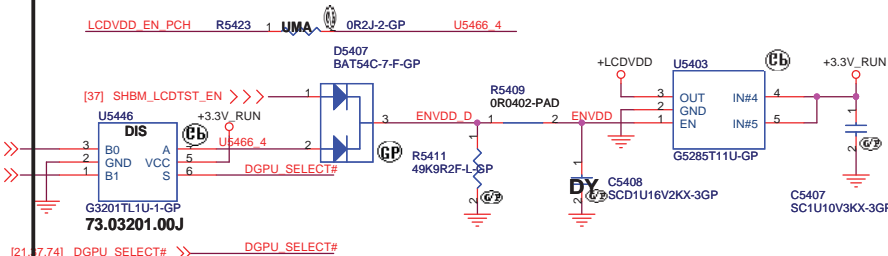
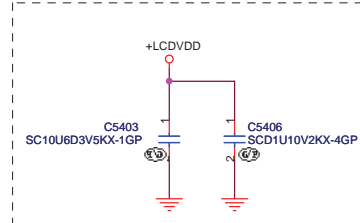
INVERTER POWER



69.50007.A41
2ND : 69.50007.A31

SSID = VIDEO

LCD POWER



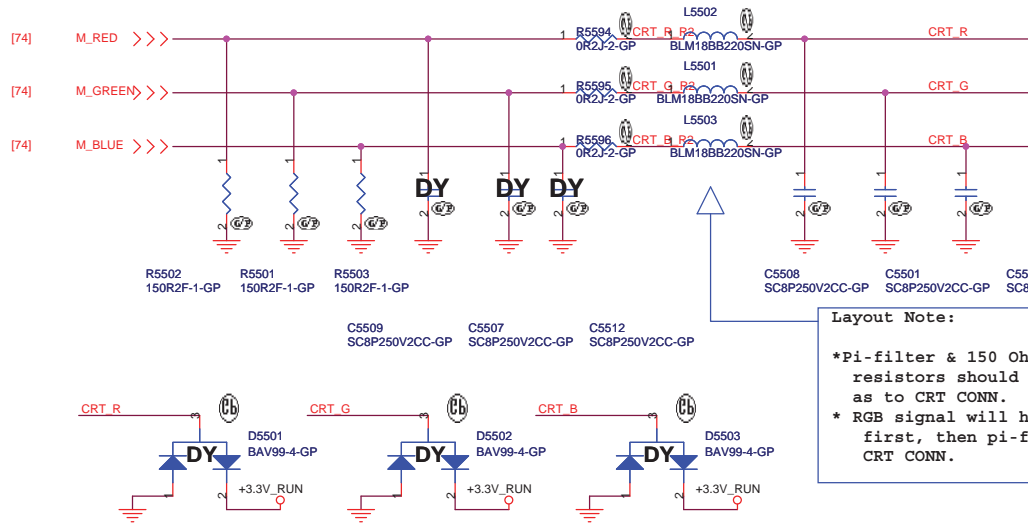
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Rev
LCD/Inverter Connector			X01
Size	Document Number	Custom	
Vostro Calpella			
Date	Monday, January 18, 2010	Sheet	54 of 91

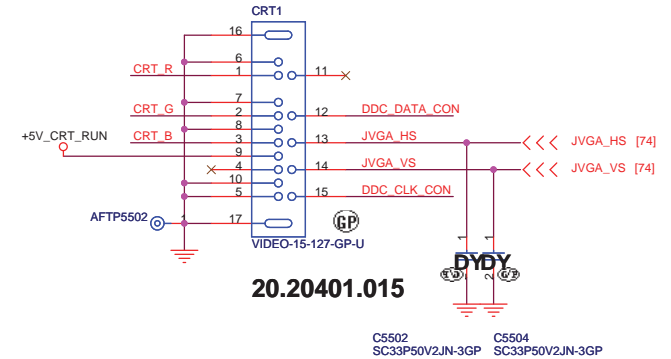
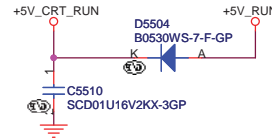
SSID = VIDEO



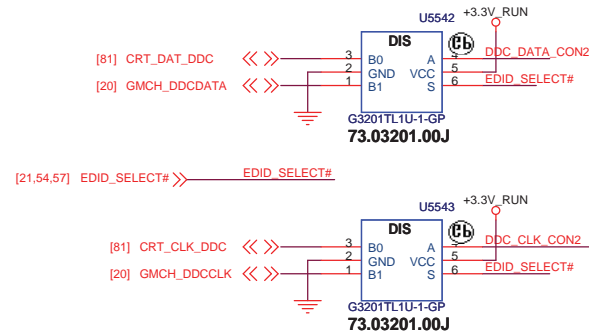
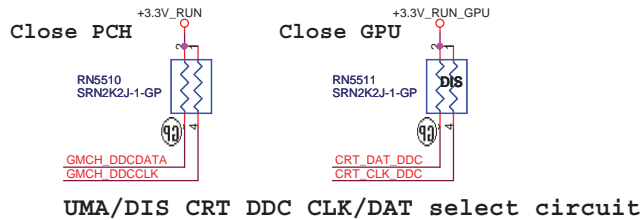
Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

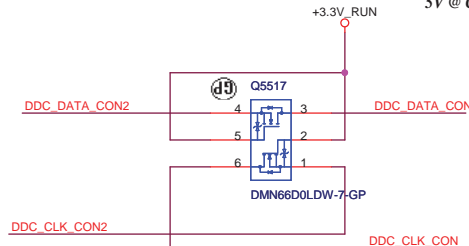
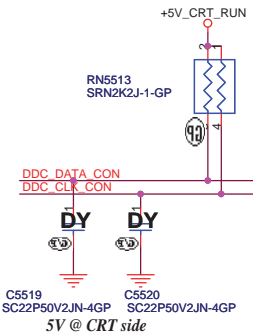
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



20.20401.015



H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)



<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.


Title: **CRT Connector**

Size: A3 Document Number: **Vostro Calpella** Rev: **X01**

Date: Monday, January 18, 2010 Sheet: 55 of 91

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size
Custom

Document Number
Vostro Calpella

Rev
X01

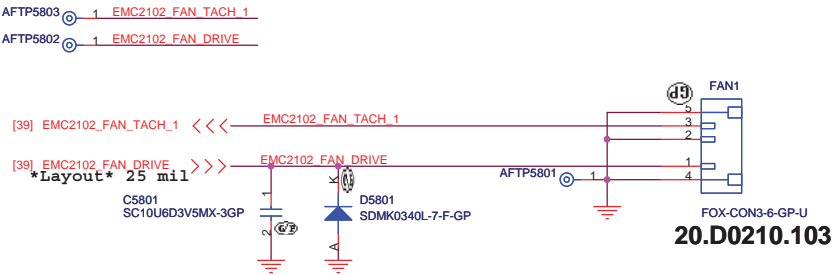
Date: Monday, January 18, 2010

Sheet 56 of 91

1

SSID = Thermal

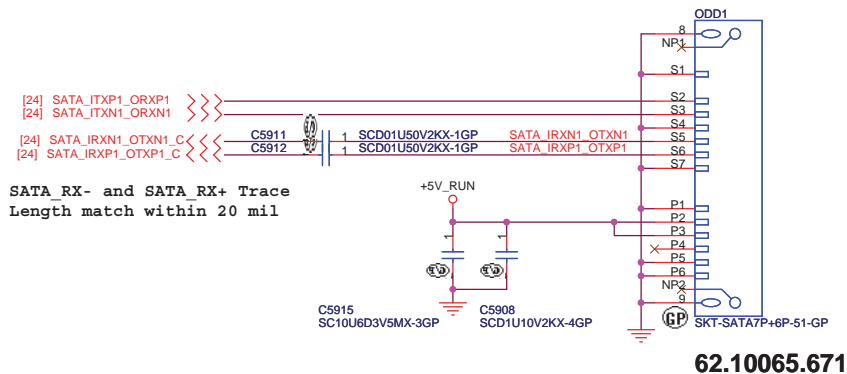
Fan Connector



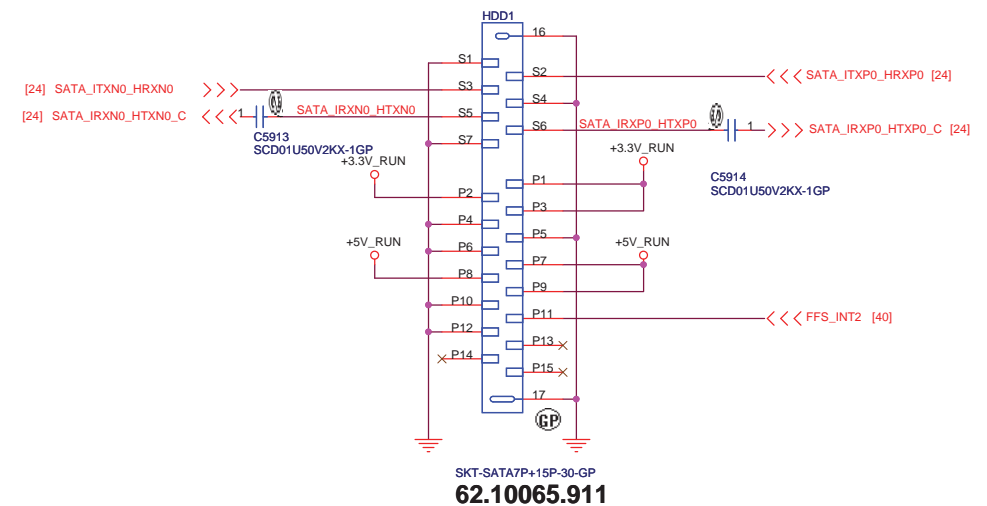
SSID = SATA

SSID = SATA

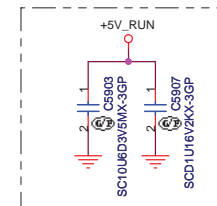
ODD Connector



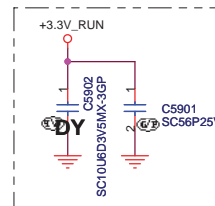
SATA HDD Connector



Close to CONN
5V power pin



Close to CONN
3.3V power pin



<Core Design>




Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Rev
HDD/ODD Connector			X01
Size	Document Number	Vostro Calpella	
A3			
Date:	Monday, January 18, 2010	Sheet	59 of 91

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010	Sheet 60 of 91
--------------------------------	----------------

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

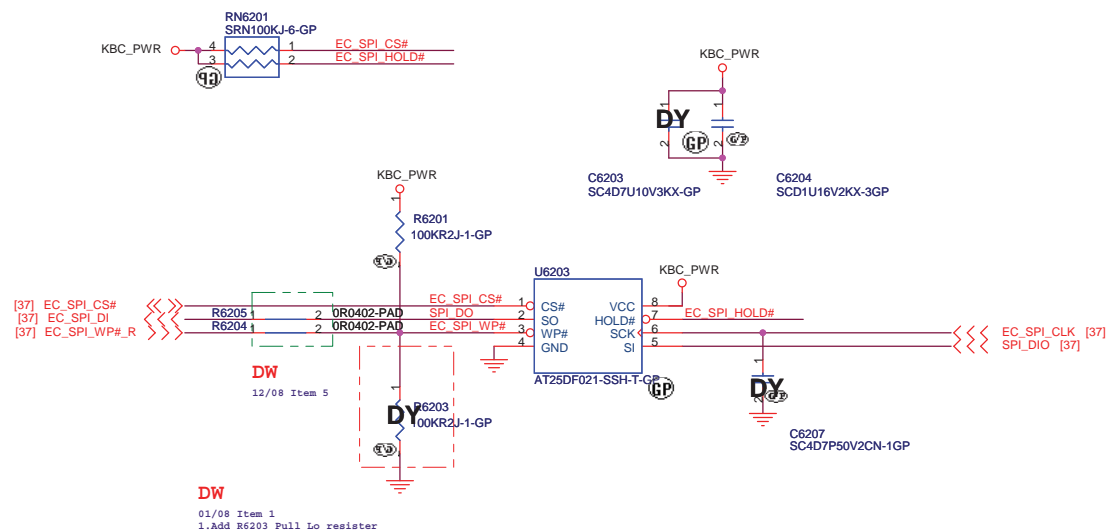
(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

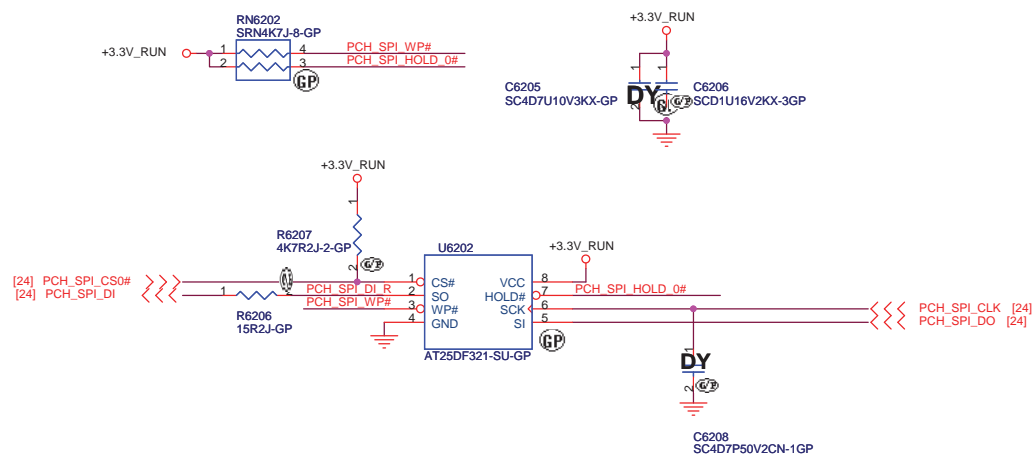
Date: Monday, January 18, 2010	Sheet 61 of 91
--------------------------------	----------------

SSID = Flash.ROM

SPI FLASH ROM (256K bytes) for KBC

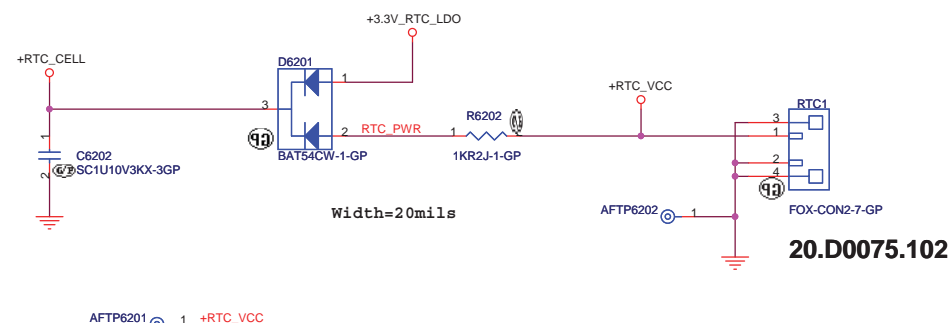


SPI FLASH ROM (4M bytes) for PCH



SSID = RBATT

RTC Connector



<Core Design>

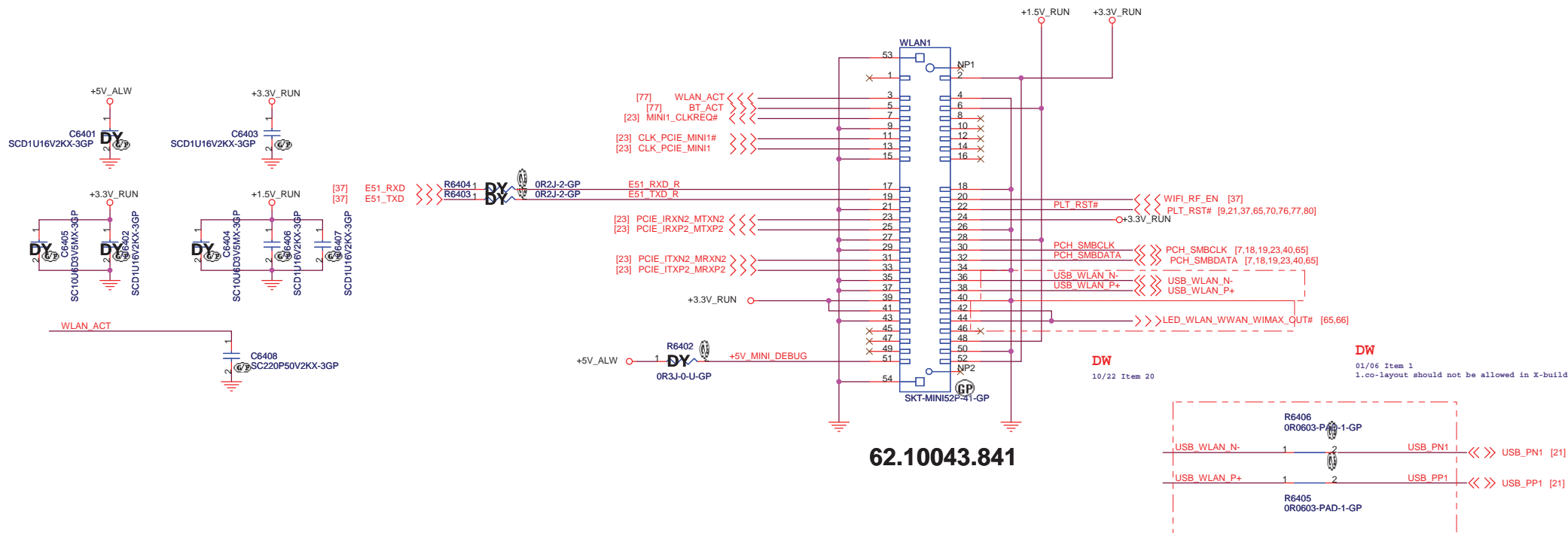


Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
EEPROM/RTC Connector		
Size A3	Document Number Vostro Calpella	Rev X01
Date: Monday, January 18, 2010	Sheet 62 of 91	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>

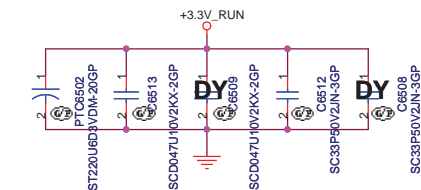
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			MINICARD(WLAN)/ITP CONN
Size	Document Number	Rev	X01
A3	Vostro Calpella		
Date:	Monday, January 18, 2010	Sheet	64 of 91

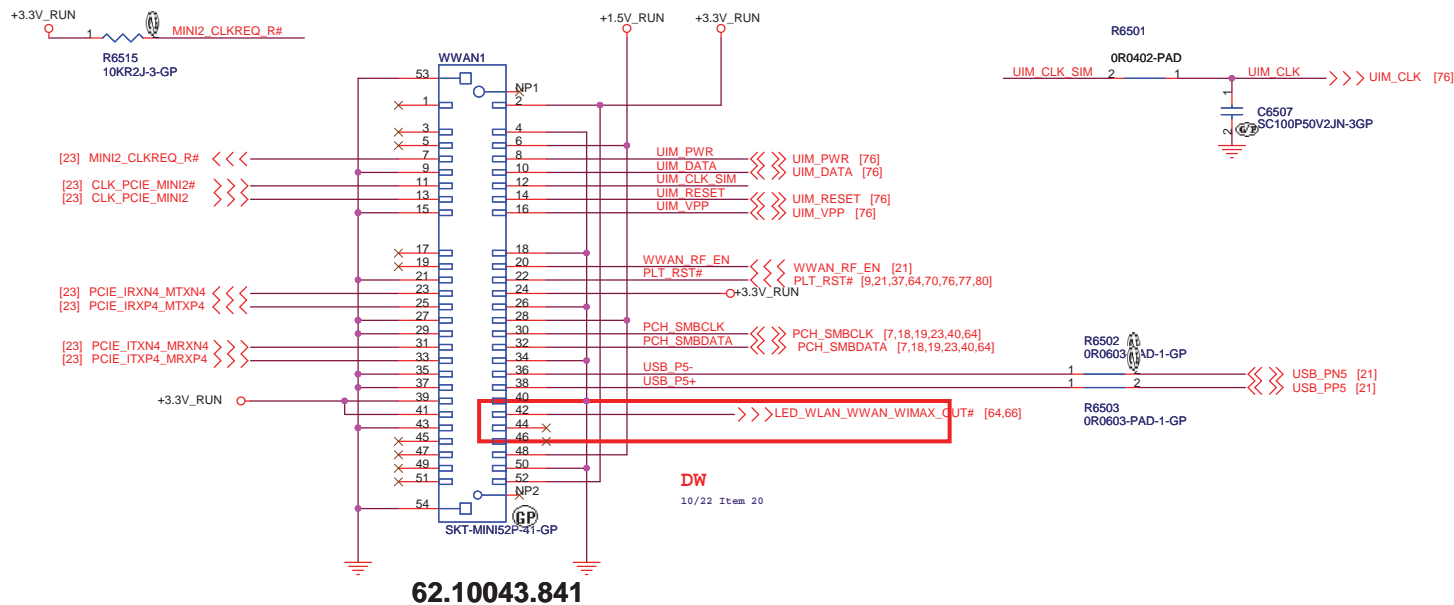
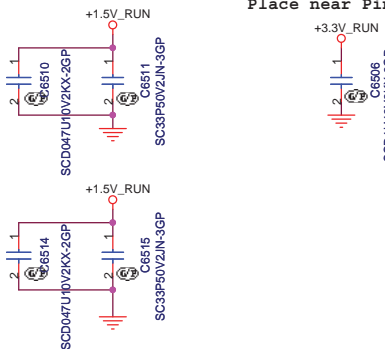
SSID = Wireless

Mini Card Connector(WWAN)

Place near MINI Card CONN



Place near Pin 24



<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN Connector

Size
A3

Document Number

Vostro Calpella

Rev

X01

Date: Monday, January 18, 2010

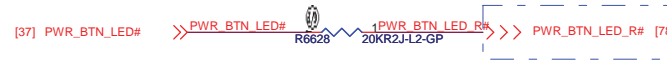
Sheet 65 of 91

For LED & Capacity board:

LED Type	Color	Power rail
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN WWAN WIMAX LED	White	RUN

PWR BTN LED

For LED & Capacity board



SCRLK LED

For LED & Capacity board:



CAPS LED



NUM LED



Remove BJT to daughter board

Bluetooth LED

For LED & Capacity board:



For IO board

LED Type	Color	Power rail
PWR LED2	White(Multi-color)	ALW
BATTERY LED2	Amber(Multi-color)	ALW
	White(Multi-color)	ALW

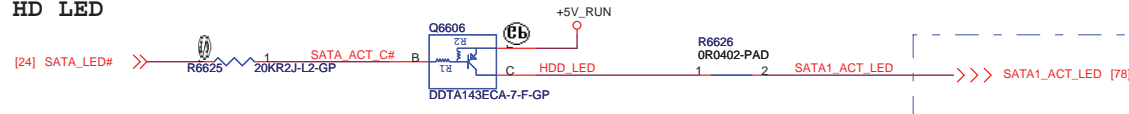
WLAN WWAN WIMAX LED

DW
10/22 Item 20



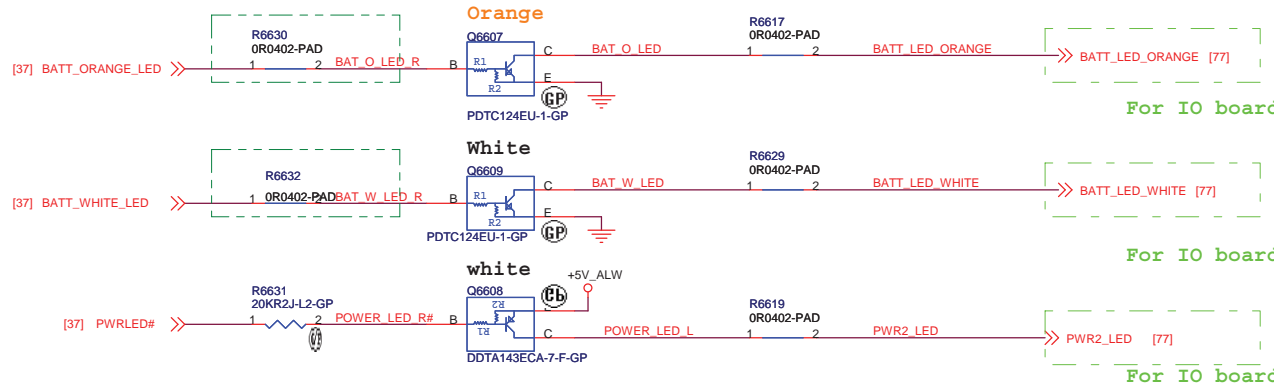
For LED&Capacity board:

HD LED



Battery & Power LED

DW
12/08 Item 5

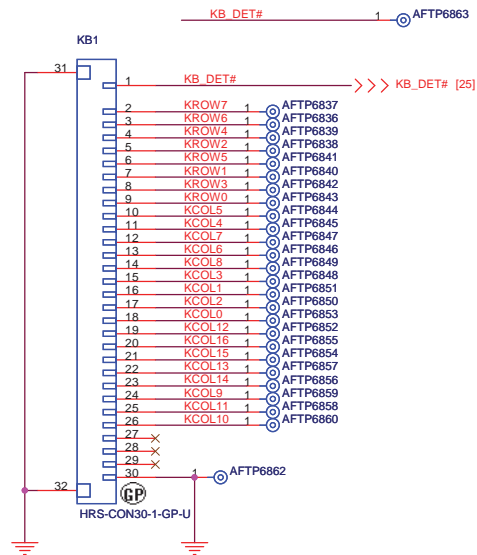


<Core Design>

(Blank)

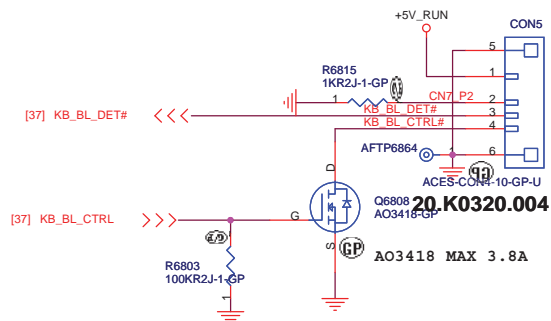
SSID = KBC

Internal Keyboard Connector



20.K0259.030

KB Backlight CONN

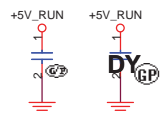


AFTP6833 1 +5V_RUN

AFTP6832 1 CN7 P2

AFTP6834 1 KB BL_DET#

AFTP6861 1 KB BL_CTRL#



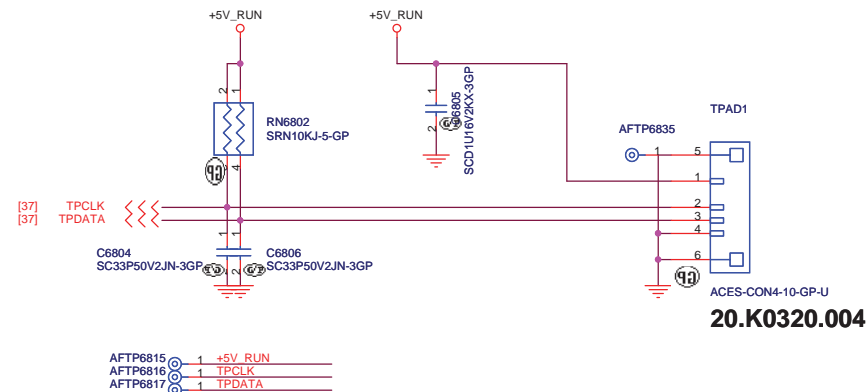
C6812 SCD1U25V2ZY-1GP

C6895 SC4D7U10V5KX-1GP

Place near CON5

SSID = Touch.Pad

TouchPad Connector

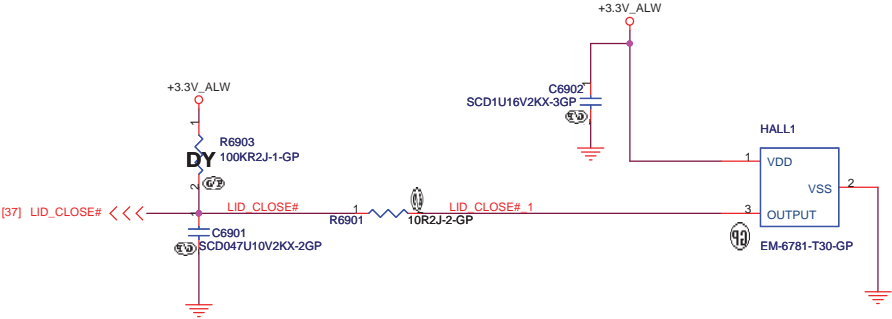


<Core Design>

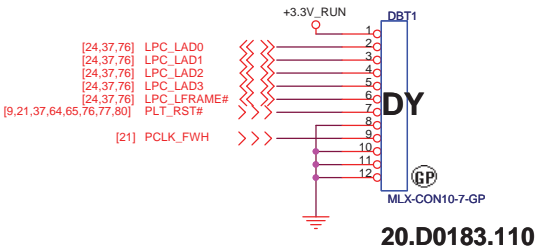
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Keyboard/Touch Pad		
Size	Document Number	Rev
Custom	Vostro Calpella	X01
Date:	Monday, January 18, 2010	Sheet 68 of 91

Hall Sensor Connector



GOLDEN FINGER FOR DEBUG BOARD




<Core Design>

(Blank)

(Blank)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

Rev

Custom

Vostro Calpella

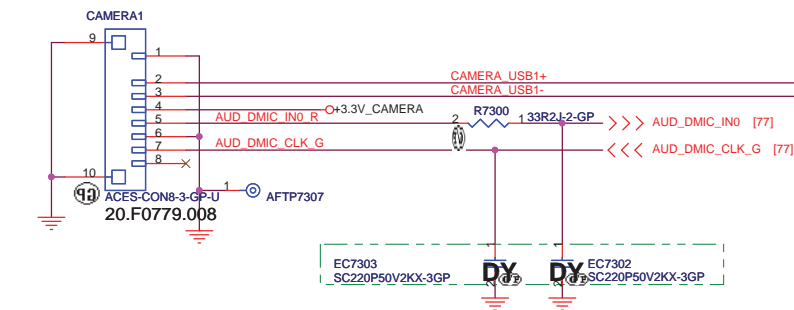
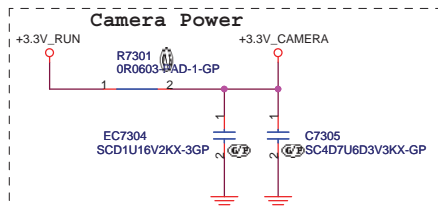
X01

Date: Monday, January 18, 2010

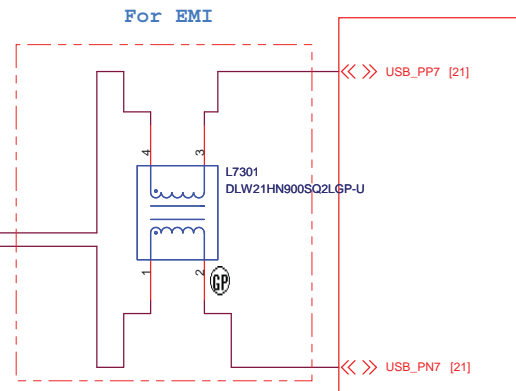
Sheet 72 of 91

SSID = User.Interface

Camera Connector



AFTP7303 1 AUD_DMIC_IN0_R
AFTP7304 1 +3.3V_CAMERA
AFTP7305 1 CAMERA_USB1-
AFTP7306 1 CAMERA_USB1+



DW
01/18 Item 1

DW
01/06 Item 1
1.co-layout should not be allowed in X-build

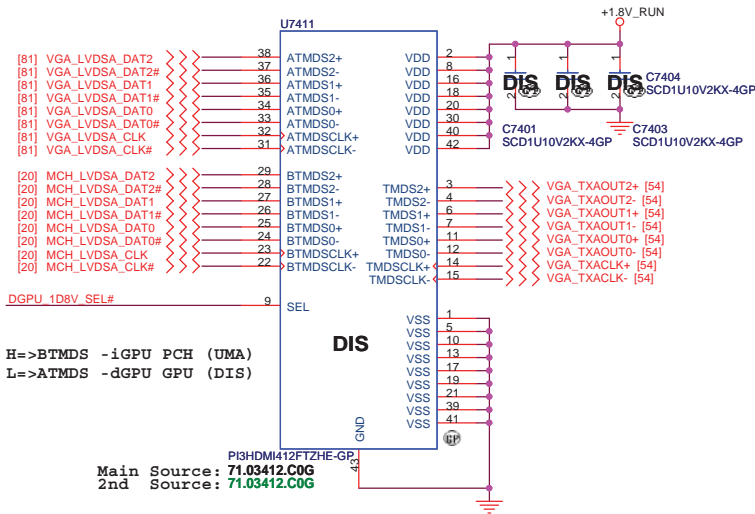
DW
12/08 Item 5

<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Camera CONN		
Size A3	Document Number Vostro Montevina Discrete	Rev X01
Date: Monday, January 18, 2010	Sheet 73 of 91	

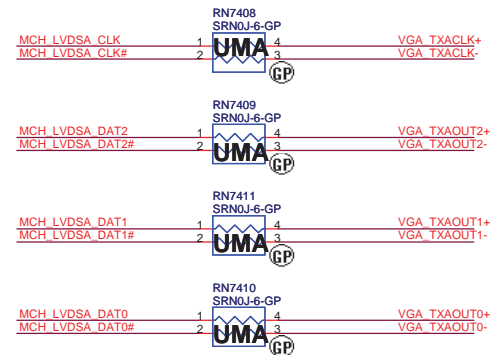
UMA/DIS LVDS signal select circuit



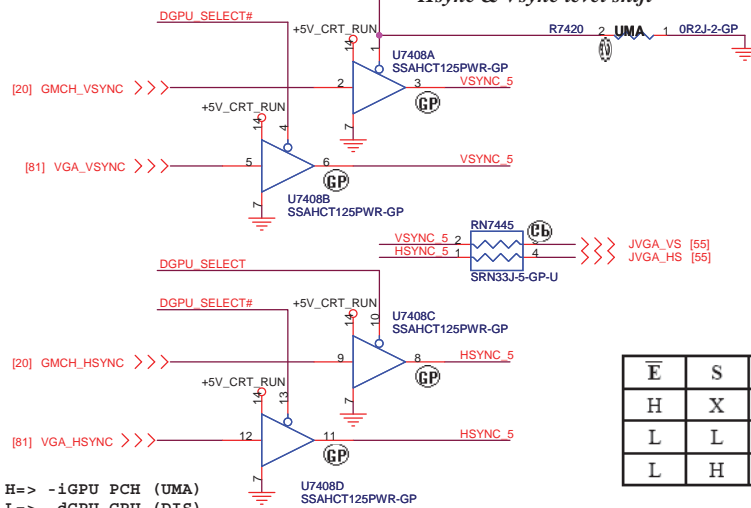
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSClk+ = ATMDSClk+ TMDSClk- = ATMDSClk- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSClk+ = High Impedance BTMDSClk- = High Impedance	TMDSn+ TMDSn- TMDSClk+ TMDSClk-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSClk+ = BTMDSClk+ TMDSClk- = BTMDSClk- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSClk+ = High Impedance ATMDSClk- = High Impedance	TMDSn+ TMDSn- TMDSClk+ TMDSClk-

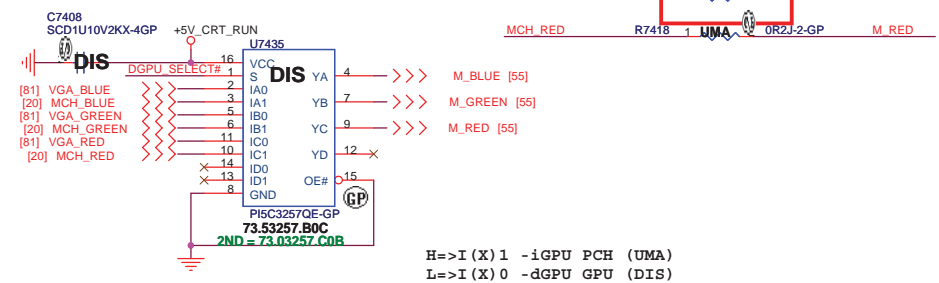
UMA LVDS signal circuit



UMA/DIS CRT Hsync/Vsync select circuit



UMA/DIS CRT signal select circuit



E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: **Swith-1**

Size: Custom Document Number: **Vostro Calpella** Rev: **X01**

Date: Monday, January 18, 2010 Sheet 74 of 91

(Blank)

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

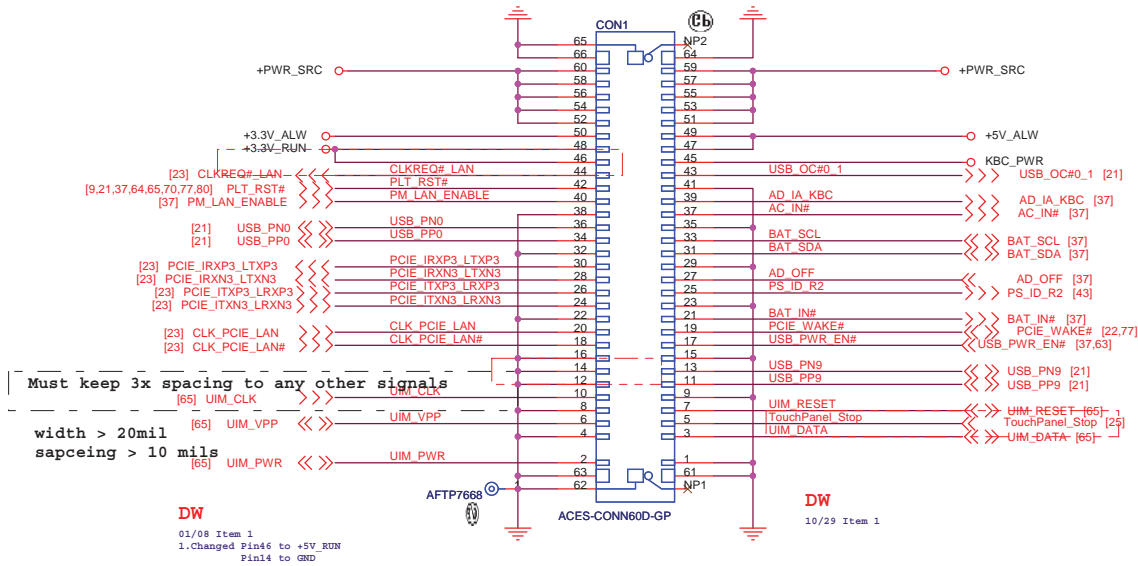
Document Number
Vostro Calpella

Rev
X01

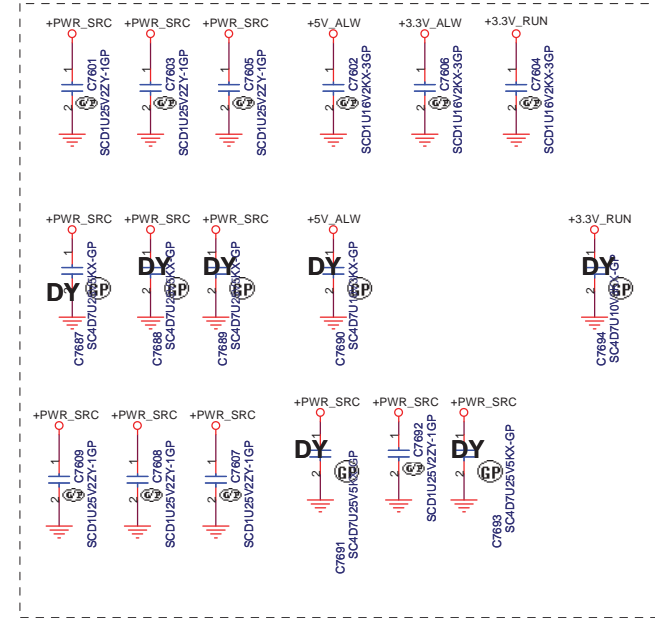
Date: Monday, January 18, 2010

Sheet 75 of 91

DC_IN board CON



Place near CON1

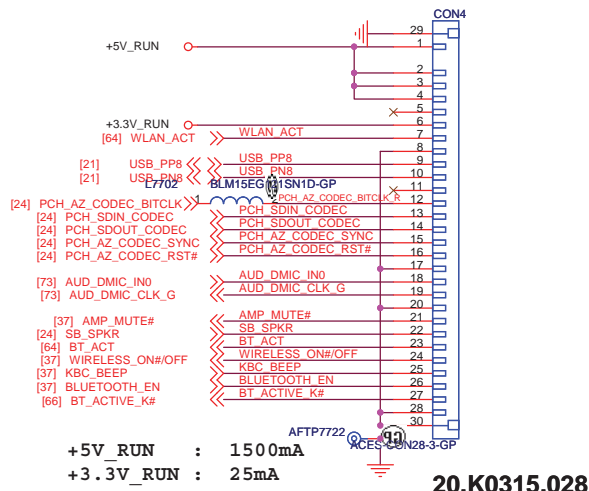


DW
01/08 Item 1
1.Remove DC-IN Board AFTP

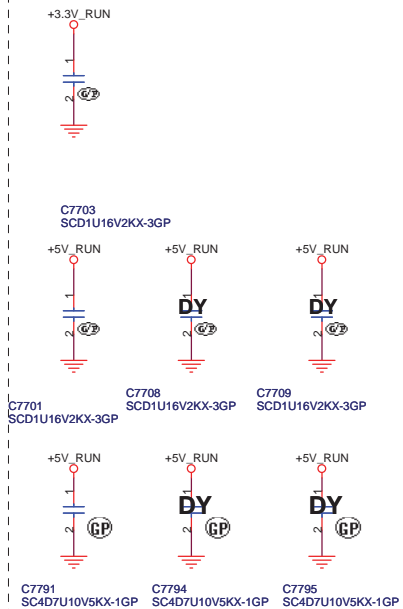
<Core Design>

SSID = User.Interface

Audio board CON

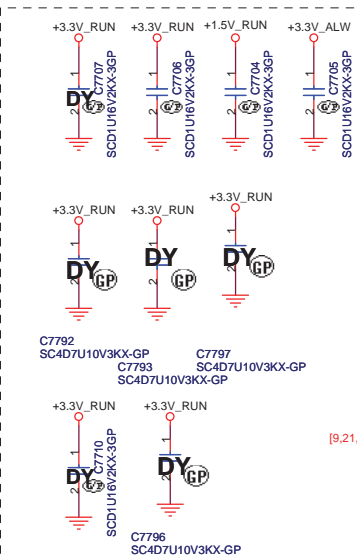


Place near CON4



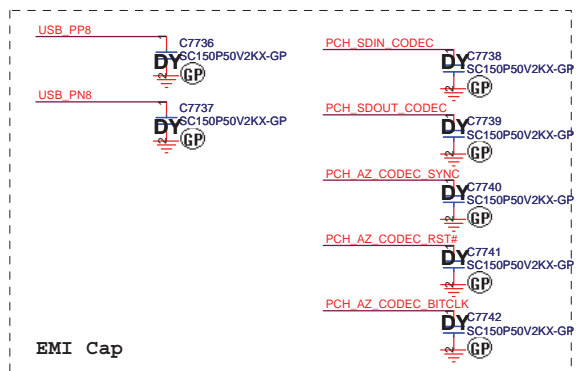
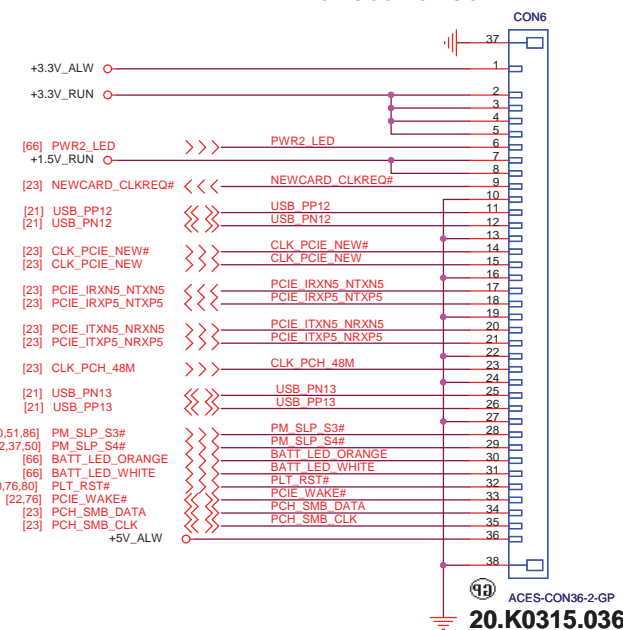
AFTP7710	1	+5V_RUN
AFTP7706	1	+3.3V_RUN
AFTP7709	1	WIRELESS_ON#/OFF
AFTP7702	1	WLAN_ACT
AFTP7703	1	BLUETOOTH_EN
AFTP7704	1	BT_ACTIVE_K#
AFTP7705	1	BT_ACT
AFTP7707	1	USB_PP8
AFTP7708	1	USB_PN8
AFTP7712	1	PCH_AZ_CODEC_BITCLK_R
AFTP7713	1	PCH_SDIN_CODEC
AFTP7714	1	PCH_SDOUT_CODEC
AFTP7715	1	PCH_AZ_CODEC_SYNC
AFTP7716	1	PCH_AZ_CODEC_RST#
AFTP7718	1	SB_SPKR
AFTP7719	1	KBC_BEEP
AFTP7720	1	AUD_DMIC_IN0
AFTP7721	1	AUD_DMIC_CLK_G
AFTP7723	1	AMP_MUTE#

Place near CON6



AFTP7758	1	+3.3V_ALW
AFTP7757	1	+3.3V_RUN
AFTP7760	1	+1.5V_RUN
AFTP7762	1	USB_PN12
AFTP7759	1	USB_PP12
AFTP7769	1	NEWCARD_CLKREQ#
AFTP7768	1	PCH_SMB_CLK
AFTP7767	1	PCH_SMB_DATA
AFTP7777	1	PM_SLP_S3#
AFTP7776	1	PM_SLP_S4#
AFTP7773	1	BATT_LED_ORANGE
AFTP7772	1	PWR2_LED
AFTP7781	1	PLT_RST#
AFTP7785	1	BATT_LED_WHITE
AFTP7787	1	+5V_ALW
AFTP7771	1	CLK_PCIE_NEW#
AFTP7770	1	CLK_PCIE_NEW
AFTP7761	1	PCIE_IRXN5_NTXN5
AFTP7765	1	PCIE_IRXP5_NTXP5
AFTP7764	1	PCIE_ITXN5_NRXN5
AFTP7763	1	PCIE_ITXP5_NRXP5
AFTP7775	1	USB_PN13
AFTP7766	1	USB_PP13
AFTP7774	1	PCIE_WAKE#
AFTP7778	1	CLK_PCH_48M

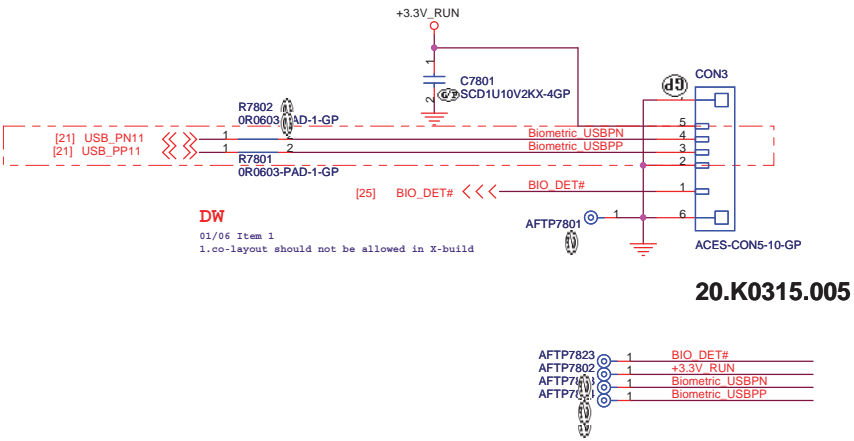
IO board CON



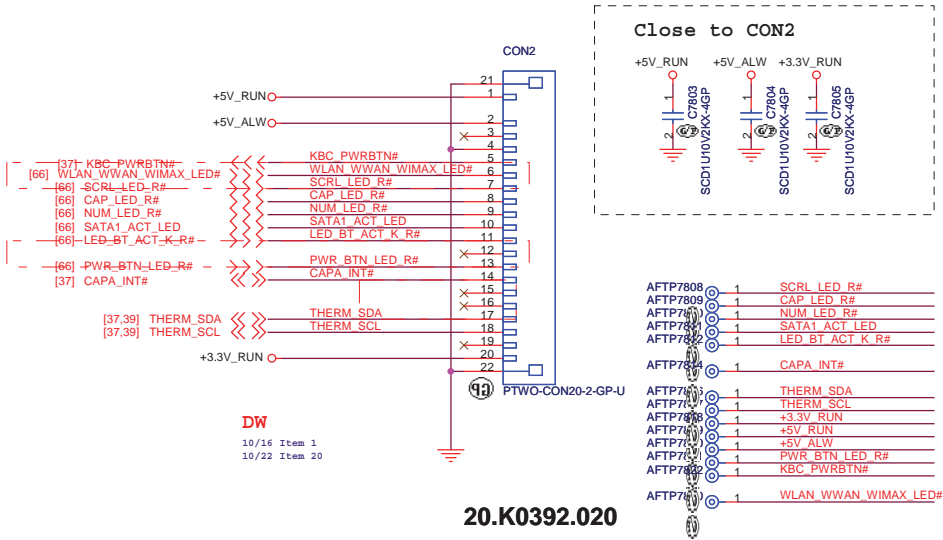
<Core Design>

DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Audio BD/IO BD CONN		
Size: Custom	Document Number: Vostro Montevina Discrete	Rev: X01
Date: Monday, January 18, 2010	Sheet: 77	of: 91

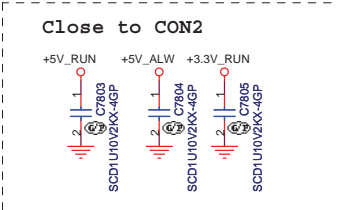
Finger Printer Connector



LED&Capacity board CONN

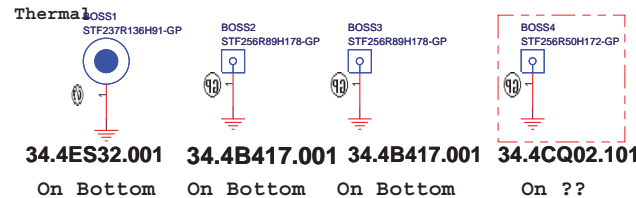


+3.3V_RUN : 3.5mA
+5V_RUN : 240mA
+5V_ALW : 80mA



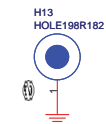
SSID = Mechanical

BOSS:



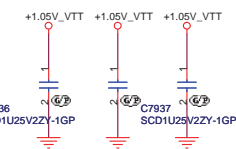
DW

12/03 Item 5

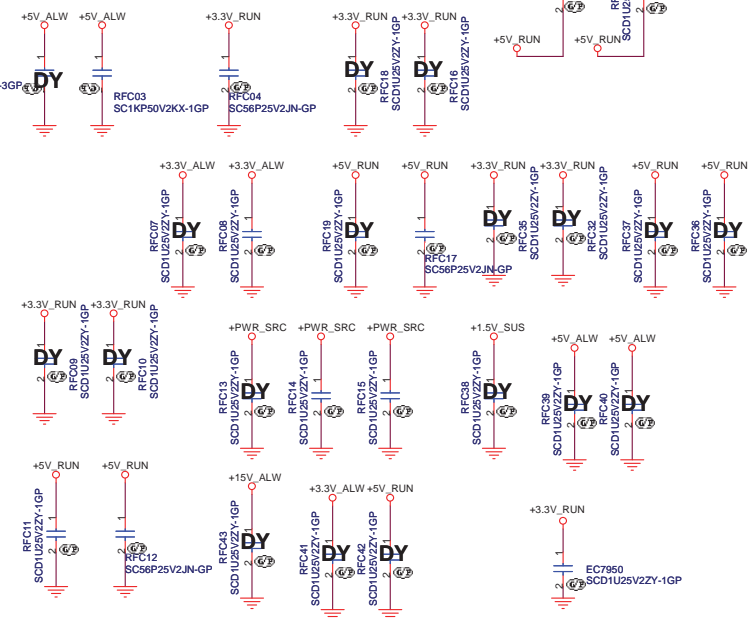


77.77777.777

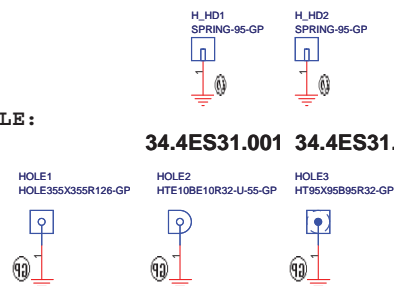
For DMI



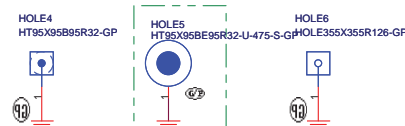
For RF Team



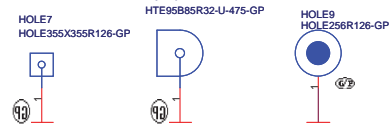
HOLE:



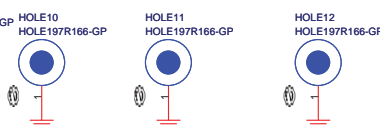
ZZ.00PAD.I71 ZZ.00PAD.K81 ZZ.00PAD.N81



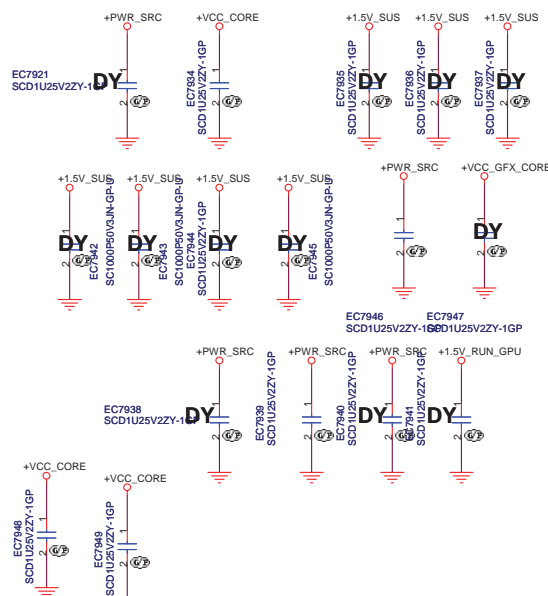
ZZ.00PAD.N81 ZZ.00PAD.Q41 ZZ.00PAD.I71



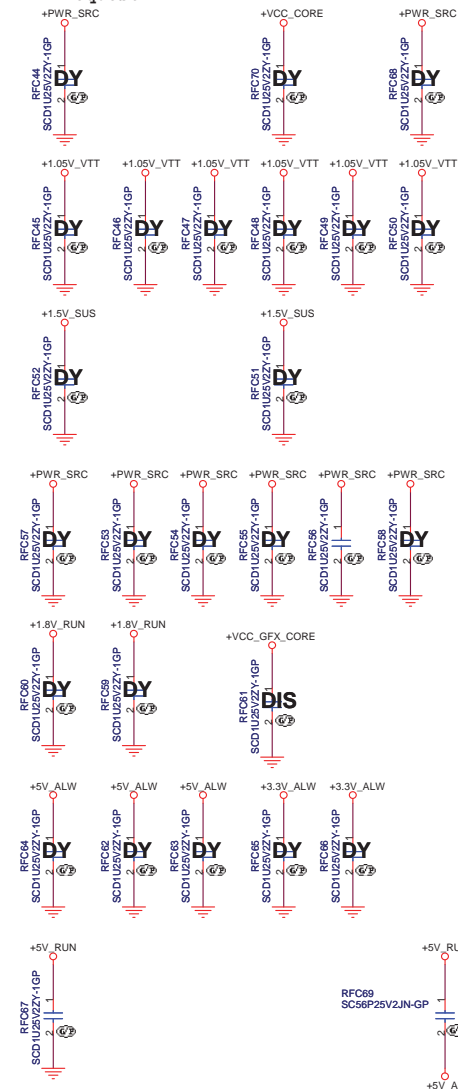
ZZ.00PAD.I71 ZZ.00PAD.N91 ZZ.00PAD.J01



34.4EM01.001 34.4EM01.001 34.4EM01.001



EMI Request



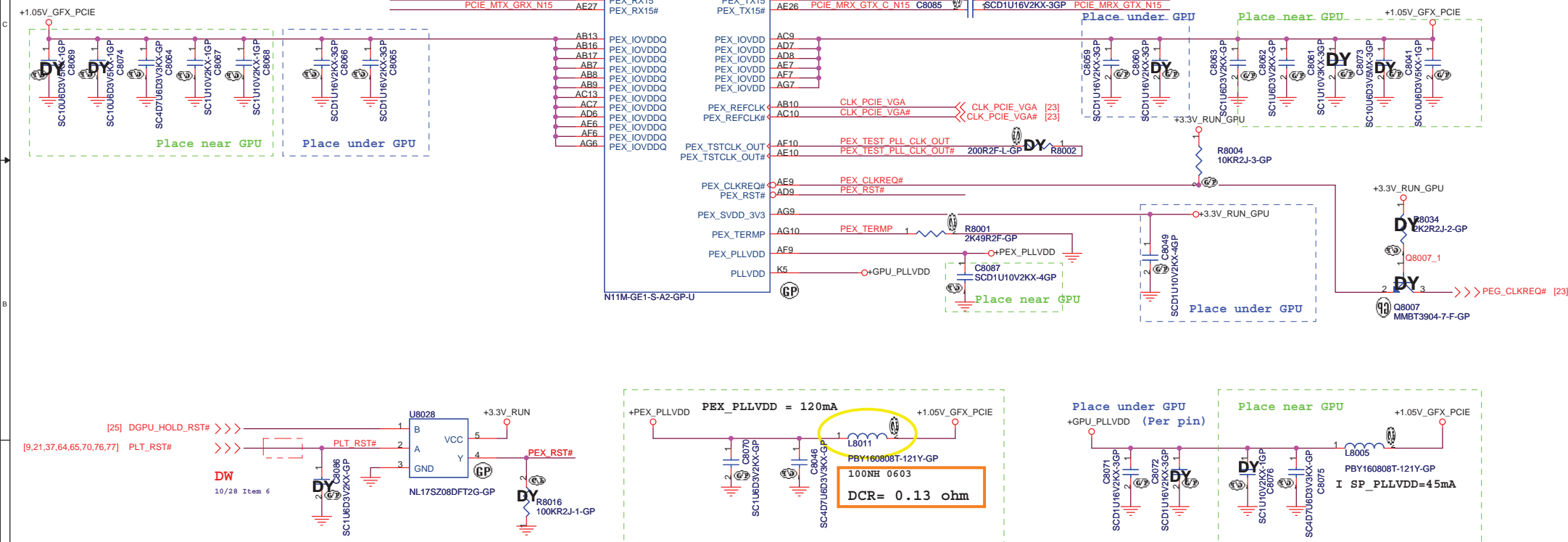
<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Miscellaneous Components			
Size	Document Number	Rev	
Custom	Vostro Calpella		X
Date: Monday, January 18, 2010		Sheet 79 of	91

SSID = VIDEO



<Core Design>



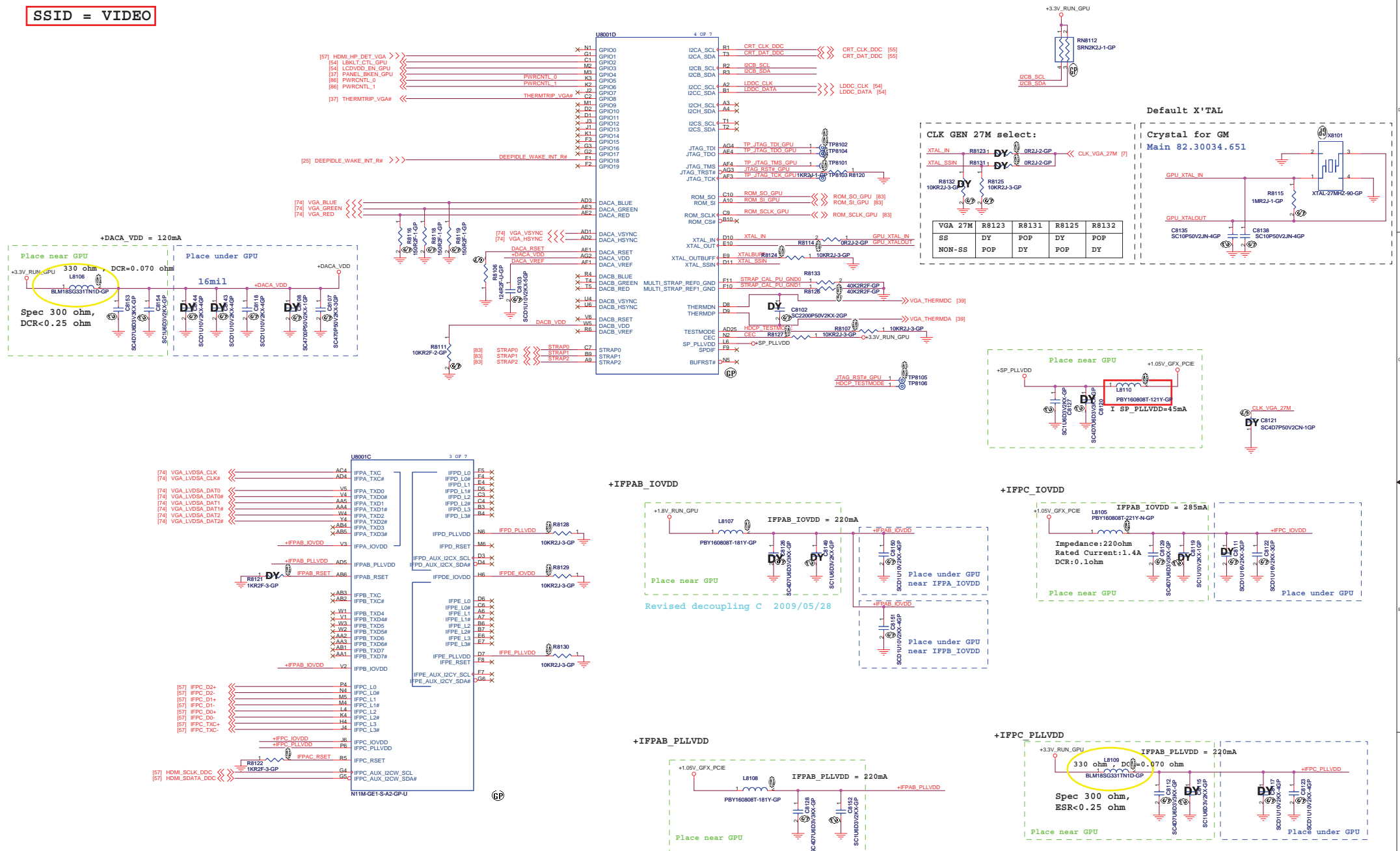
Title _____

VGA-PCIE/LVDS(1/4)

Size A3	Document Number	Rev
------------	-----------------	-----

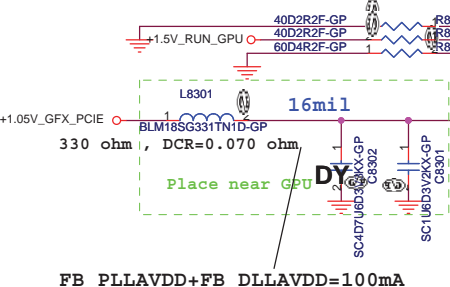
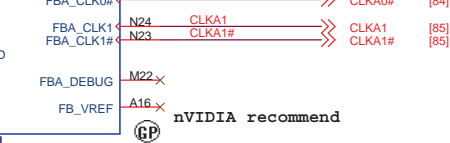
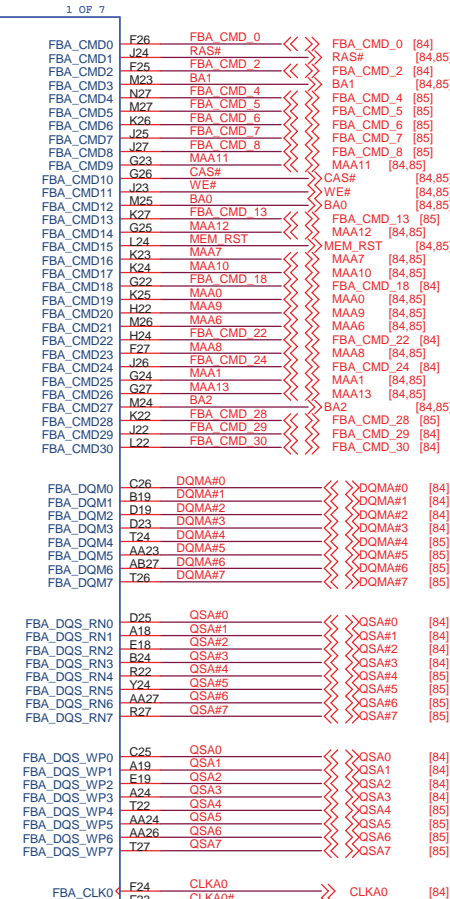
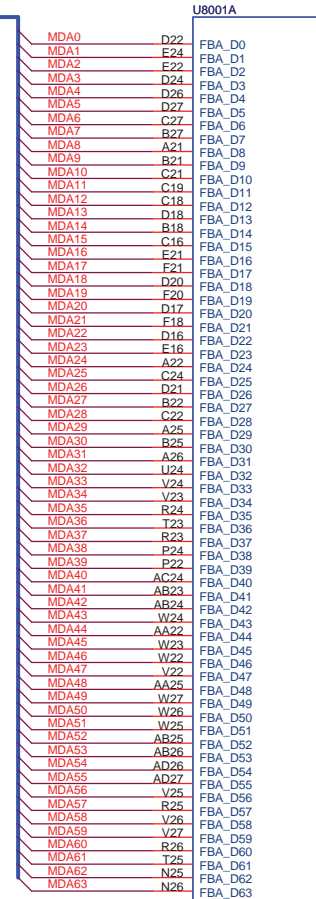
Date: Monday, January 18, 2010 Sheet 80 of 91


```
SSID = VIDEO
```

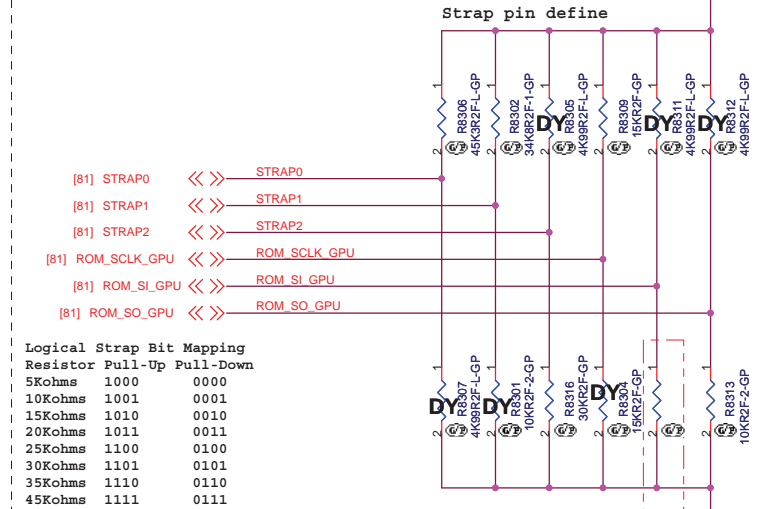


SSID = VIDEO

[84,85] MDA[0..63] <<



Strap pin resistor need use 1% resistor (NV Design Guide)



Strap0 Strap1 Strap2
 USER_BIT0 1 3GIO_PADCFG_LUT_ADR0 0 PCI_DEVID_0 1
 USER_BIT1 1 3GIO_PADCFG_LUT_ADR1 1 PCI_DEVID_1 0
 USER_BIT2 1 3GIO_PADCFG_LUT_ADR2 1 PCI_DEVID_2 1
 USER_BIT3 1 3GIO_PADCFG_LUT_ADR3 1 PCI_DEVID_3 0

EDID is used Reserved N11M-GE1 GPU Device ID=0x0A75

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)

RAM_CFG[3:0]	Config	FB_BUS Width	Definitions
0000			
0001			
0010	64MX16 DDR3 64Bit	Hynix	
0011	04MX16 DDR3 64Bit	Samsung	Default
0100			
0101			
0110			
0111			

If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K

SUB_VENDOR XCLK_417 PEX_PLL_EN_TERM
 0 No VBIOS ROM 0 277MHz(POR) 0 Disable (POR)
 1 BIOS ROM present 1 Reserved 1 Enable

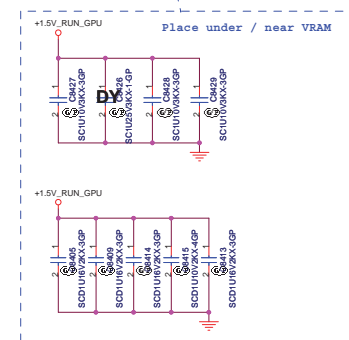
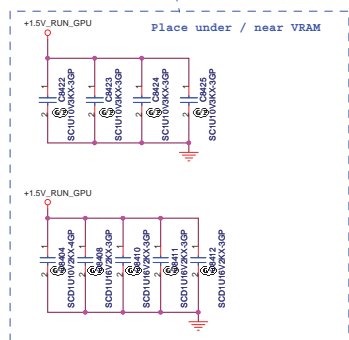
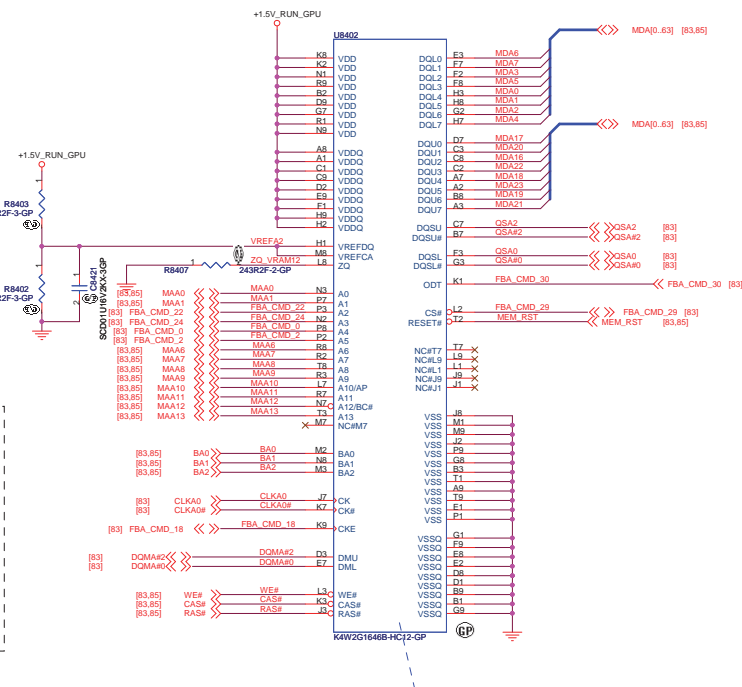
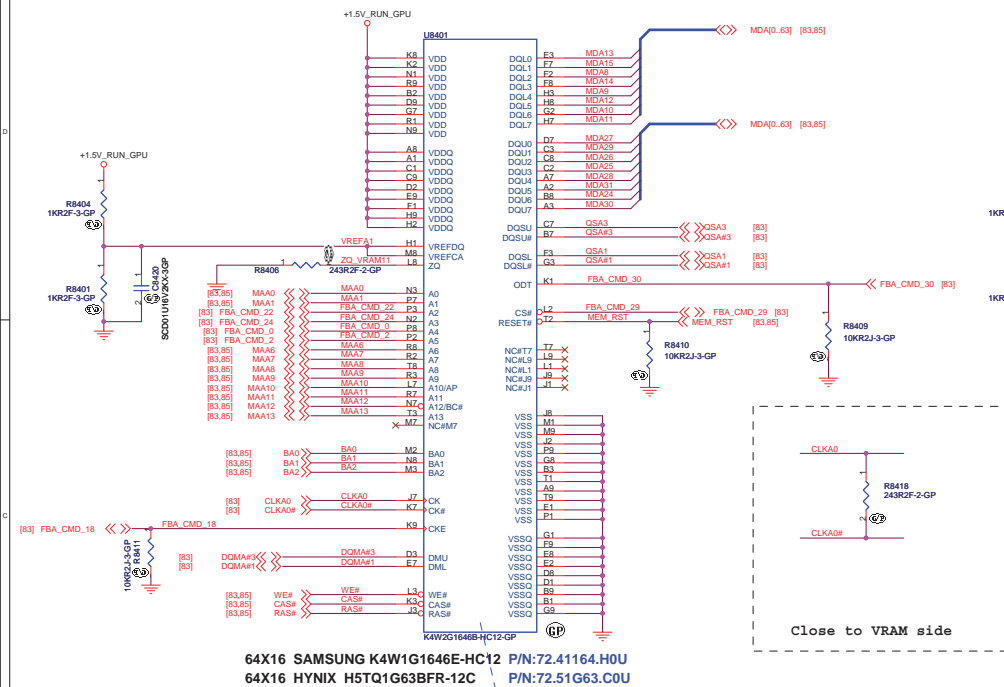
3GIO_PADCFG USER[3:0]
 0000 Desktop 1111 Use EDID to detect panel settings
 1110 Notebook (POR)

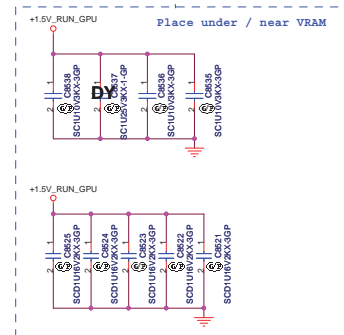
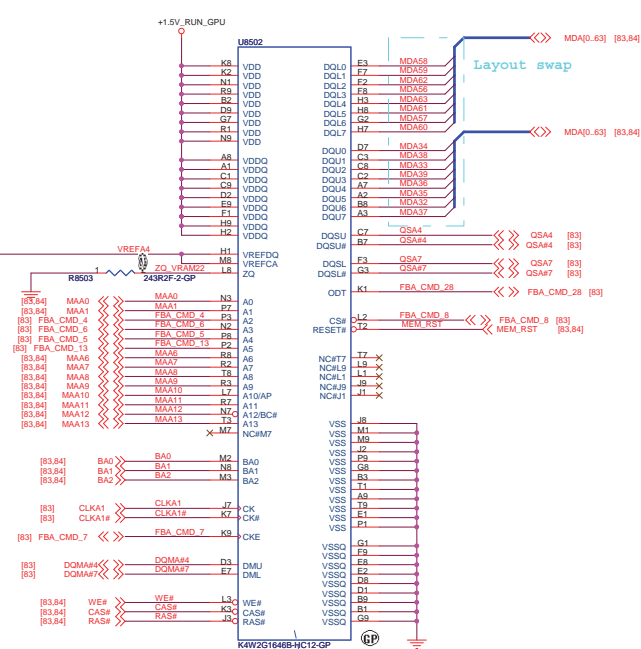
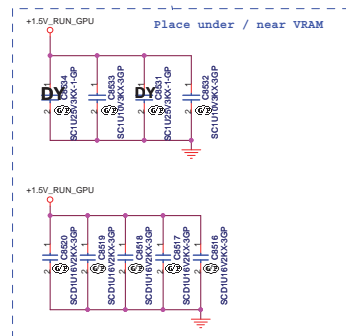
SLOT_CLOCK_CFG
 0 GPU and MCH do not share a common reference clock
 1 GPU and MCH share a common reference clock (POR)

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichu,
 Taipei Hsien 221, Taiwan, R.O.C.

Title
VGA-MEMORY/STRAPS(4/4)
 Size A3 Document Number **Vostro Calpella** Rev X01
 Date: Monday, January 18, 2010 Sheet 83 of 91

SSID = VIDEO





SSID = PWR.Plane.Regulator_GFX

$$V_{out} = 0.704V * (R1 + R2) / R2$$

DIS
Thermal Design Current = 12.9A
Max Current = 16.77A
18.45A < OCP < 21.81A

Frequency setting
470K --> 290KHz
200K --> 340KHz
100K --> 380KHz
39K --> 430KHz

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
L	H	1.03V
L	L	0.85V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEP5X0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/ 14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

<Core Design>

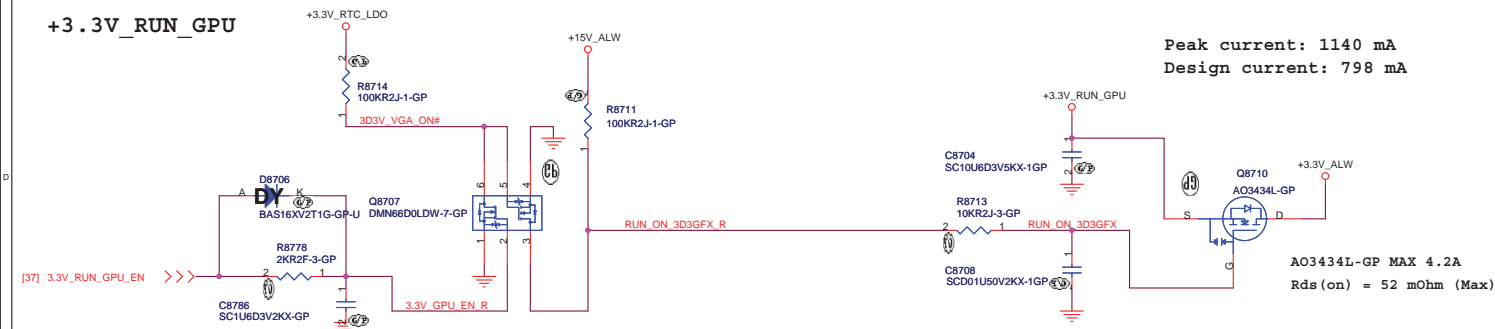
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51218 +VCC GFX CORE**

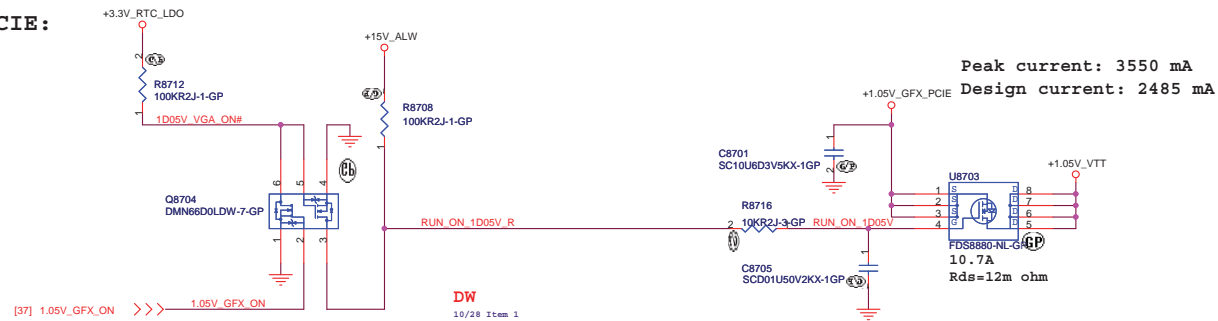
Size: Custom Document Number: **Vostro Calpella (Discrete)** Rev: **X01**

Date: Monday, January 18, 2010 Sheet: 86 of 91

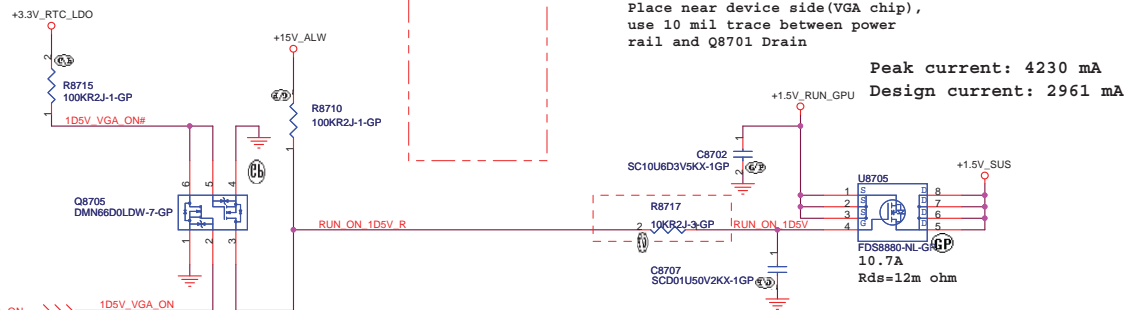
+3.3V_RUN_GPU



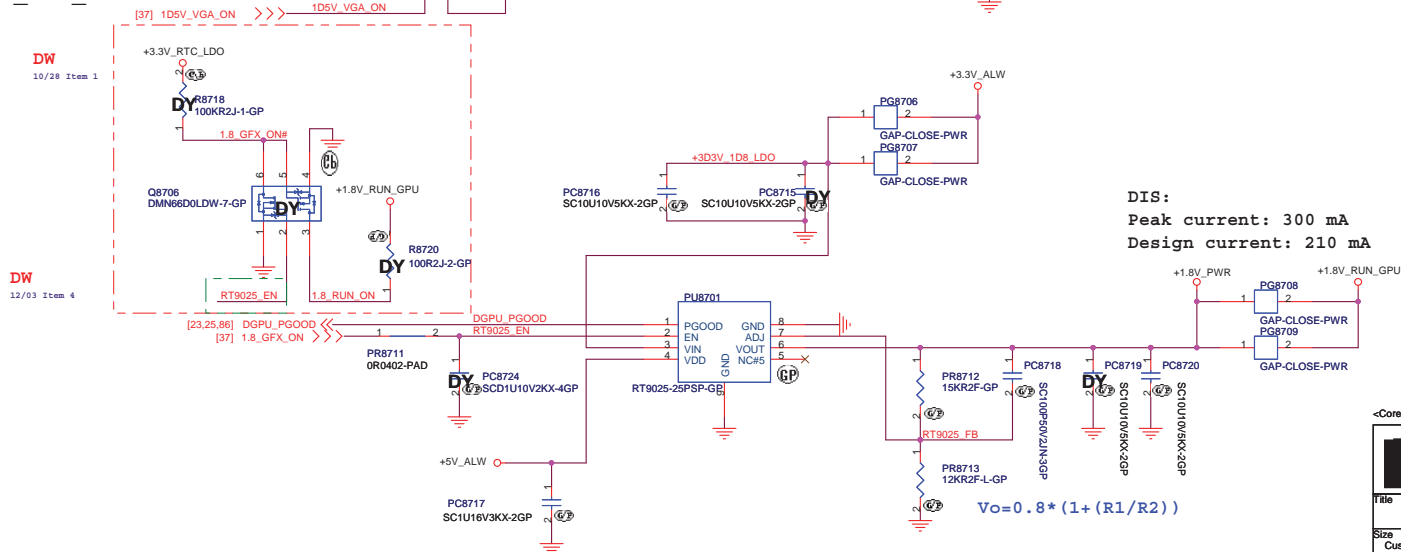
+1.05V_GFX_PCIE:



+1.5V RUN GPU:



+1.8V_RUN_GPU



Peak current: 1140 mA
Design current: 798 mA

Peak current: 3550 mA
Design current: 2485 mA

Peak current: 4230 mA
Design current: 2961 mA

DIS:
Peak current: 300 mA
Design current: 210 mA

<Core Design>

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				LDO 1.8V			
Size	Document Number						Rev
Custom	Vostro Calpella						XC
Date:	Monday, January 18, 2010				Sheet	87	of 91

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/15	X01	1	25	Swapped Q2515 C,E Pin	For correct.	EE
		2	All	Combine pull-up/down resistors from single to series resistor	For save more part counts	EE
		3	37	Update 10mW circuit.	For DC mode power consumption can be less than 10mW under S5.	EE
		4	22	Add U2213,R2221	Added 3v/5v S5 power good to control resume reset sequence circuit prevent RTC data loss.	EE
		5	51	stuffed PC5105 with 1uF	For power sequencing of +1.8V_RUN , Delay timing	EE
		6	23	Added 25M Crystal	For DCI (DisplayClock_Integration)	EE
		7	79	Added BOSS4	For Steady the thermal module	EE
		9	All	BOSS1 from 34.4W005.001 to 34.4CQ03.101 CON3 from 20.K0315.005 to 20.K0293.006 CON4 from 20.K0315.028 to 20.K0275.028 CON6 from 20.K0315.036 to 20.K0276.036 DM1 from 62.10017.U81 to 62.10017.P31 DM2 from 62.10017.U71 to 62.10017.Q31 HOLE1 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE2 from ZZ.00PAD.K81 to ZZ.00PAD.E11 HOLE3 from ZZ.00PAD.N81 to ZZ.00PAD.D71 HOLE4 from ZZ.00PAD.N81 to ZZ.00PAD.D71 HOLE5 from ZZ.00PAD.K11 to ZZ.00PAD.E11 HOLE6 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE7 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE8 from ZZ.00PAD.N91 to ZZ.00PAD.D31 HOLE9 from ZZ.00PAD.J01 to ZZ.00PAD.D11 LCD1 from 20.F1093.040 to 20.F1555.030 TPAD1 from 20.K0320.004 to 20.K0265.004	For ME request Changed connect PN:	ME
		1	37,87	Removed CAPA_RST# from Capacity board		EE
				Added Switch Baord Detection circuit	For software request.	EE
		1	77	Reversal CON6 Pin 36 <-> 1 ; 35 <-> 2	For new connect pin define.	EE
		2	9,27	Changed RN907,L2701,L2704	For update components	EE
		3	74	Swapped the RN7408,RN7409,RN7410,RN7411	For Layout request.	EE
2009/10/16						
2009/10/19						

<Core Design>




Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Change List - EE(1)		
Size Custom	Document Number Vostro Calpella	Rev X01
Date: Monday, January 18, 2010	Sheet 88 of	91

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/19	X01					
		2	81	Remove R8149	For EMI team request	EMI
			21	PCLK_FWH、CLK_PCI_FB、PCLK_KBC、PCLK_TPM reserve by pass cap		
2009/10/22			23	CLK_PCH_48M reserve by pass cap		
			23	Romove R2350 and C2324		
			37	Romove R3726 and C3704		
			79	Reserve +PWR_SRC to GND cap		
		3	79	Add EC7934 0.1u in +VCC_CORE	For EMI team request	EMI
2009/10/23				Add EC7911 0.1u +1.5V_SUS to GND cap*1		
				Add EC7935,EC7936 0.1u +1.5V_SUS to GND cap*2		
				Add EC7937 0.1u +1.5V_SUS to GND cap*1		
				Add EC7938 0.1u +PWR_SRC to GND cap*1		
				Update TR6304,TR6305 p/n to 68.00201.141		
		4	73	Move EC7302	For EMI team request	EMI
			79	dummy 0.1u x 2 in green area 6135,195 ----EC7939,EC7940		
				dummy 0.1u cap in red area 1755,4435 ----EC7941		
				dummy 1000p in green area 5225,6950----EC7942		
				dummy 1000p in green area 3780,6180----EC7943		
2009/12/08 2009/12/09	SC SC			dummy 104p and 1000p in green area 5385,7010---EC7944,EC7945		
				dummy 0.1u in green area 3400,6300---EC7946		
				dummy 0.1u in green area 1240,4035--EC7947		
		55		add damping 33ohm on R,G,B Singel---R5594,R5595,R5596		
		1	79	mount EC7948,EC7949,EC7934	For RF Team request	RF
		1	73	mount LECM2012H-900QT-GP in L7301	For EMI team request	EMI
		2	24,77	change R2405 from 10 ohm to 56 ohm and mount 120 ohm bead bead p/n:BLM15EG121SN1 L7702		
		3	73	mount 220p cap on EC7302 and EC7303		
		4	79	Add EC7950		

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Change List - EMI&RF	
Size	Document Number	Rev	
Custom	Vostro Calpella	X01	
Date: Monday, January 18, 2010		Sheet 90	of 91

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/22	X011	1	46	PR4604,PR4605 --> 4.7ohm for RT, 0 ohm for TI	Change PU4603 from TPS51125 to RT8205B	Power Team
				PR4622 --> 820k ohm for RT, DY for TI		
				PR4616 --> ASM for RT, DY for TI		
				PR4617 --> DY for RT, ASM for TI		
2009/10/29			53	PC5307 change to 68nF for Intel spec	Improve Jitter issue	Power Team
		2	50	Add 4.7uF at +PWR_SRC_1D5V		